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A COMPARISON OF RATE 1/n CONVOLUTIONAL CODES OVER A SIMULATED NOISY CHANNEL USING THE VITERBI DECODING ALGORITHM

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NAVAL POSTGRADUATE SCHOOL Monterey, California



THESIS

A COMPARISON OF RATE 1/n CONVOLUTIONAL CODES OVER A SIMULATED NOISY CHANNEL USING THE VITERBI DECODING ALGORITHM

by

James Howard Haney

December 1974

Thesis Advisor:

G. H. Marmont

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The application of error detection and correction codes has advanced markedly with the advent of digital technology. However, the strides made towards employing the techniques, encoding and decoding, properly have been rather limited by the Naval forces in the United States. This paper develops a computer program, which if utilized properly, would aid in deciding what error correcting scheme is best suited for a specific channel.



20. The results obtained from testing a rate 1/n convolutional code, over a simulated channel, using a Viterbi decoder shows that this is an effective analysis procedure. Though the test runs were lengthy, much of the time required was for noise simulation. This would not be a factor if actual channel noise recordings had been available.

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A Comparison of Rate 1/n Convolutional Codes Over a Simulated Noisy Channel Using the Viterbi Decoding Algorithm

bу

James Howard Haney
Captain, United States Marine Corps
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Submitted in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL December 1974

Theris Allie

ABSTRACT

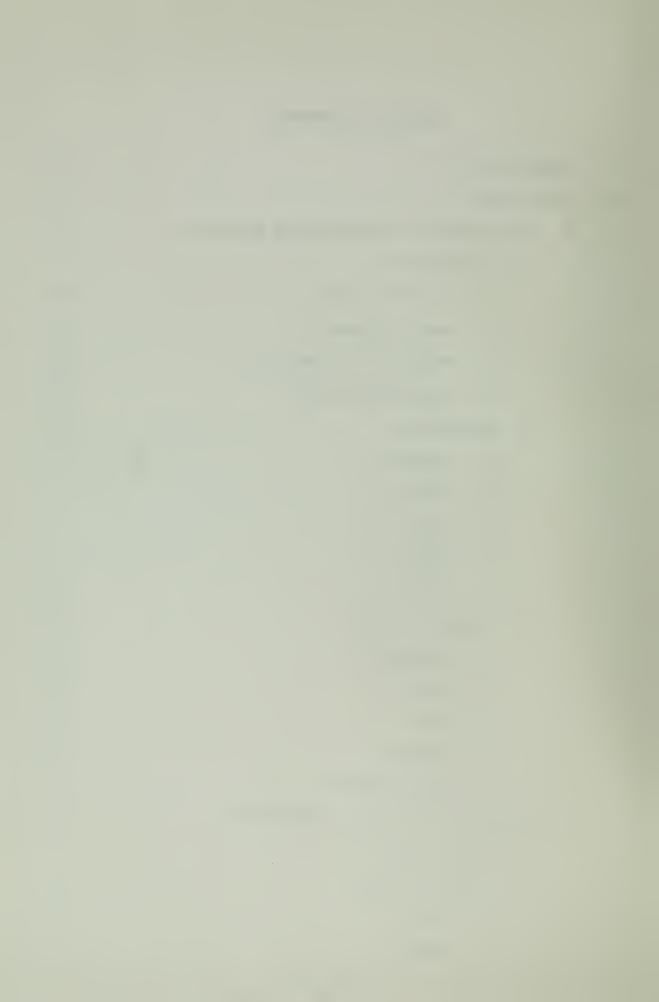
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TABLE OF CONTENTS

ı.	INTR	ODUC	TION		10
II.	BAC	KGRO	UND	·	13
	Α.	PRI	NCIPI	LES OF CONVOLUTIONAL ENCODING	15
		1.	Des	cription	15
			a.	Code Rate (k/n)	20
			b.	Memory Length (M)	20
			c.	Constraint Length (K)	20
			d.	Free Distance (d _f)	20
		2.	Prop	perties	25
			a.	Property 1	25
			b.	Property 2	25
			c.	Property 3	27
			đ.	Property 4	28
			e.	Property 5	28
		3.	Rep	resentation	29
			a.	Polynomial	29
			b.	Matrix	31
			c.	Tree	33
			d.	Trellis	35
			e.	State Diagram	38
	в.	PRI	NCIP	LES OF VITERBI DECODING	40
		1.	Des	cription	41
		2.	Imp	lementation	43
			a.	Step 1	44
			b.	Step 2	44

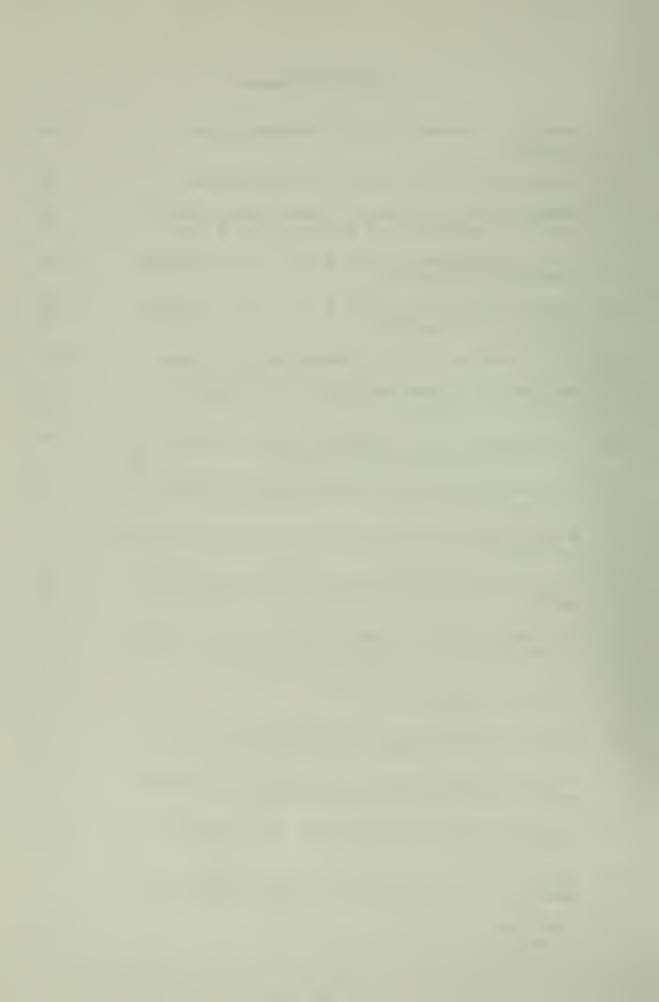


	c. Step 3 (Figure 14)	46
	d. Subsequent Steps	48
III. C	OMPUTER PROGRAM ·	52
. А	. CHANNEL NOISE	52
	1. Quantization	52
	2. Random Numbers	52
	3. Noise Generation	53
	4. Perturbation	55
В	. PROGRAM FLOW	62
IV. R	ESULTS AND CONCLUSIONS	65
A	. BEST CODE DETERMINATION	65
В	. DECODER PARAMETER VARIATIONS	71
С	. DISCUSSION AND CONCLUSIONS	71
APPENDI	X A	75
APPENDI	х в	78
APPENDI	x c	82
APPENDI	x D	84
APPENDI	X E	90
APPENDI	X F	96
LIST OF	REFERENCES	98
DISTRIBU	UTION LIST	99



LIST OF FIGURES

1.	Model of a One-Way Digital Communication System.	14
2.	Conventional (n,k) Convolutional Encoder	18
3.	Representation of the i^{th} Input Section of a Rate k/n convolutional Encoder (1 \leq i \leq k).	19
4.	Mealy Configuration of a M = 2, n = 2, Binary Convolutional Encoder.	21
5.	Moore Configuration of a K = 3, n = 2, Binary Convolutional Encoder.	22
6.	Block Diagram of Basic Communication System	26
7.	Polynomial Representation of a Generalized Generator Sequence.	30
8.	Generalized Matrix Representation of a Rate 1/2 Convolutional Encoder (K=3).	34
9.	Tree Representation of Convolutional Encoder in Figure 5.	36
LO.	Trellis Representation of Convolutional Encoder in Figure 5.	37
11.	State Diagram Representation of Convolutional Encoder in Figure 5.	39
L2.	An Example of Remerging Path in Trellis Diagram of Convolutional Encoder (K=3).	42
L3.	Present State Initialization for Viterbi Decoding Algorithm.	45
L4.	Next State Tables at the Completion of the First Shift of 2-Bits Into the Decoder.	47
15.	The Next State Tables for the Second Through Fifth 2-Bit Shift into the Decoder.	49
16.	The Next State Table After 18 Shifts and the Decoded Output to that Point.	50
17.	Comparison of Congruential Random Number Generator (10 ⁵ bits) with Poisson Distribution.	54
18.	Simulated Noise (Q = 1, λT = 9.8) Vs Poisson Distribution (λT = 9.8).	56

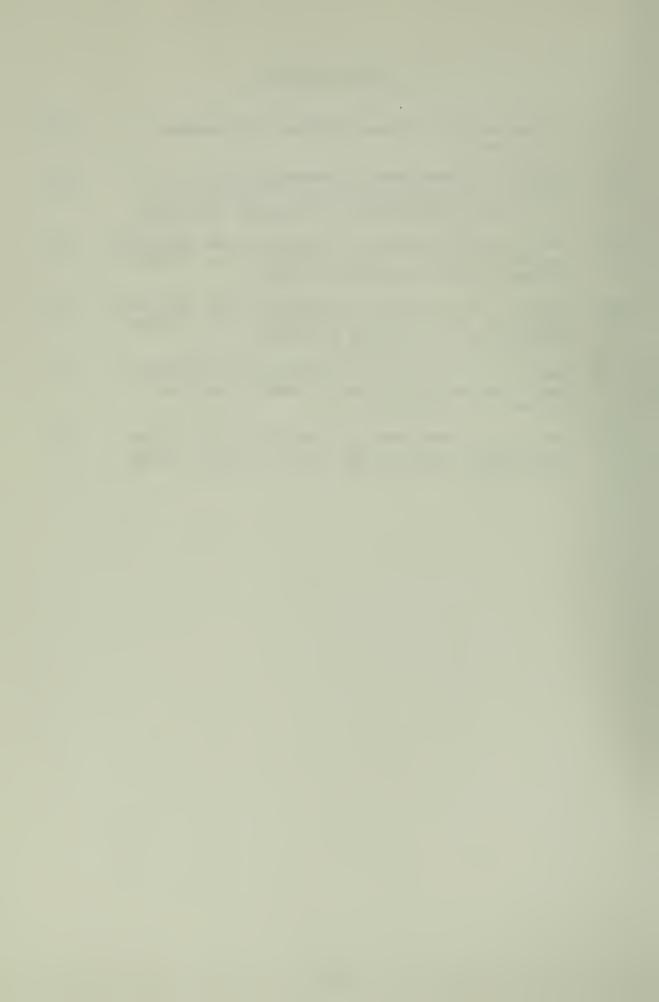


19.	Simulated Noise (Q = 1, λT vs Poisson Distribution (λ	,	57
20.	Simulated Noise (Q = 2, λT vs Poisson Distribution (λ		58
21.	Simulated Noise (Q = 2, λT vs Poisson Distribution (λ		59
22.	Simulated Noise (Q = 3, λT vs Poisson Distribution (λ		60
23.	Simulated Noise (Q = 3, λT vs Poisson Distribution (λ'		61
24.	Block Diagram of Program F	low.	64
25.	The measure of average erroinformation input rate to is similar to Shannon's Re	a channel (figure	67



LIST OF TABLES

ı.	Determination of Free Distance for Encoder in Figure 5.	24
II.	Results of Test Runs to Determine the Generator Sequences (n = 2, K = 3) Yielding the Minimum Probability of Decoded Bit Error.	68
III.	Results of Test Runs to Determine the Generator Sequences (n = 2, K = 4) Yielding the Minimum Probability of Decoded Bit Error.	69
IV.	Results of Test Runs to Determine the Generator Sequences (n = 3, K = 3) Yielding the Minimum Probability of Decoded Bit Error.	70
v.	Results of Test Runs for Variation in Receiver Quantization (Q) Using the Best Codes from Tables II, III, IV.	73
VI.	Results of Test Runs for Variation in Decoder Constraint Length (DCL) Using the Best Codes from Tables II, III, IV.	74



I. INTRODUCTION

The distortion of a digital transmission, caused by noise, may require that techniques be used allowing for the detection and eventual correction of errors. In digital communications, the most significant performance parameter from either a bit or message standpoint is that of probability of error. A means of minimizing the probability of error is therefore essential to effective communication.

Error detection and correction was given great impetus by Shannon's paper of 1948, [Ref. 7], which extended the promise of reliable recovery of digital data perturbed by noise (Shannon's Second Theorem). The noisy coding theorem provides that messages can be transmitted with arbitrarily small error if the source rate is no more than the channel capacity. While this sets a goal and the conditions necessary to attain it, the precise method for obtaining a specific scheme was not set forth. However, Shannon did use a random coding scheme in proving this theorem. As was shown by Rice in 1950, [Ref. 6], following Shannon's example, choosing codewords randomly leads to the result that as the code becomes very long, channel capacity is approached and

¹ Channel capacity is the maximum average information input to a channel, which means it is properly matched to the channel less the average uncertainty at the receiver due to channel noise.



the probability of error can be made to decrease exponentially with code length. But choosing codewords randomly is not a practical scheme.

Until the 1960's the application of channel coding theory was slow in its development. The establishment of digital circuit technology and the realization of a theoretical channel (satellite communication; AWGN) provided a powerful stimulus for the utilization of practical error detection and correction techniques. The technological improvements have continued until today fairly large memories are held by small chips, and the components needed to implement powerful coding schemes are available in reduced sizes and at reasonable prices.

The objective of this paper is to demonstrate the benefits derived from a minicomputer (DEC PDP-11/40) simulation of channel noise applied to a specific error detection and correction scheme. This simulation allows for the determination of a probability of bit error for a specifiable noise density. Results from the simulation are then used to determine statistical trends of a particular error correction technique for various internal coding parameters.

The error detection and correction scheme chosen by the author is the Viterbi decoding, [Ref.3], algorithm on a rate 1/n convolutional code. Both the encoding and decoding technique are of current interest in extraterrestrial communications, with the Viterbi algorithm being principally considered for satellite communications. Therefore, in



order to provide a complete presentation, the scope of this thesis will encompass the basic principles of convolutional encoding and Viterbi decoding, as well as the structure of the simulation program, results and conclusions.

All programming was accomplished on the DEC PDP-11/40 in machine language, thus presenting the opportunity to gain valuable insight into the computer structure while completing this thesis.



II. BACKGROUND

Digital communication systems (figure 1) are usually designed to minimize the probability of error of the received data (bits), introduced by noise (gaussian, burst, fading, multipath, etc.). Thus, error detection and correction may be varied according to the degree and type of noise. There are two common forms of error protection: (1) retransmission and (2) controlled redundancy. The first may be applied to systems which are not critically affected by the ensuing delay, whereas the second does not require significant delays. This thesis deals with the latter in an attempt to gain statistical knowledge of the particular coding scheme (controlled redundancy) under study.

Controlled redundancy techniques are commonly divided into two groups: (1) block codes and (2) convolutional (tree) codes. Again, owing to the characteristics of the channel, one of these two codes may be chosen, along with a suitable decoding scheme, to achieve the desired probability of error. A decoding scheme for block codes is batch oriented, as is its encoding, using definite algebraic operations related to the segmented structure of the code. On the other hand, convolutional codes are decoded by a statistical procedure due to its continuous (bit by bit) nature.



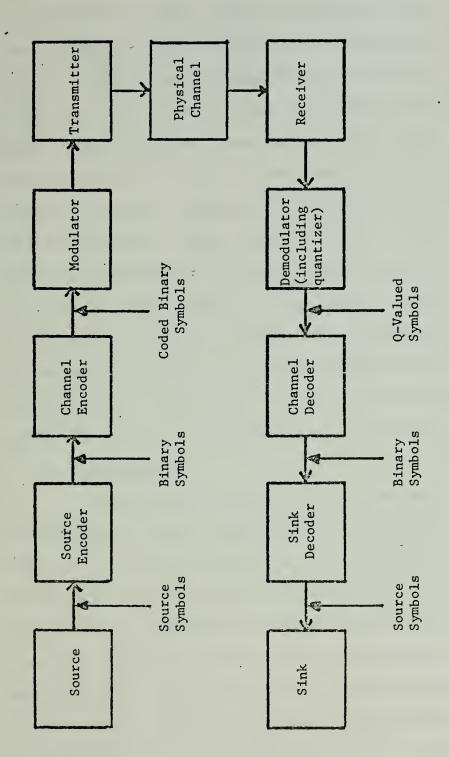
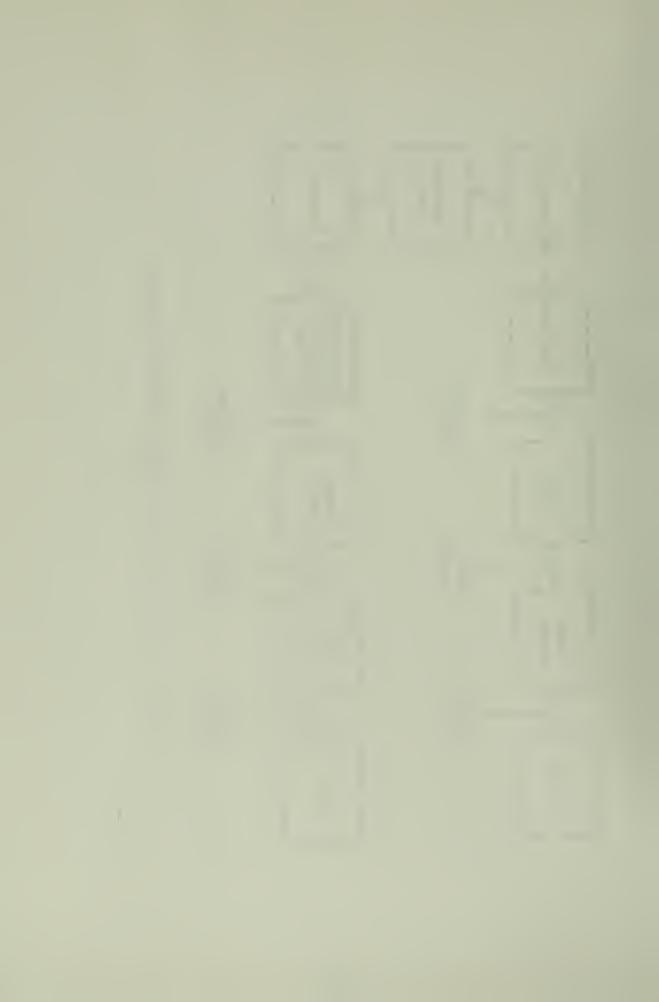


Figure 1. Model of a One-Way Digital Communication System.



A. PRINCIPLES OF CONVOLUTIONAL ENCODING

In 1955, P. Elias first proposed the use of convolutional (tree) codes for the discrete time memoryless channel, [Ref 2]. This technique extended the promise of providing a class of codes (linear) whose performance would prove superior to that of block codes of the same length, [Ref. 9]. The development of these codes also gave promise of providing for a decoder complexity increasing no more than linearly with block length and/or encoder memory. These conjectures have been verified, for the most part, by such contributors as Fano, Reiffen, Forney and Berlekamp. [Ref. 4]

Since convolutional codes form a definite discipline in coding theory, there are some aspects that will require clarification in conjunction with the implementation of the code. The next few subsections will accomplish this task.

1. Description

The process of block encoding segments (blocks) of an indefinite length input sequence into code blocks proceeds in a discrete manner, i.e., the contents of one block has no bearing on the encoding of another block. The code blocks may be completely changed from the input block or they may include the input block with check bits determined by a definite algorithm. However, when an input sequence is processed through a convolutional encoder the input/output is continuous (sequential bit to bit dependence in the encoder) and the output is generated at a specifiable number of code bits for each encoder input bit.



The term "convolutional" originates from the observation that the encoded sequence can be regarded as a convolution² of the input sequence with related generator sequences. An example of such a procedure is the binary convolution (denoted by *) of two sequences, \underline{x} and \underline{g} , where + and \cdot are binary addition and multiplication, respectively.

Input sequence:

$$\underline{x}(t_0) = (x_0 x_1 x_2 x_3 x_4 \dots) = (1 \ 0 \ 1 \ 1 \ 0 \dots);$$

Generator sequence:

$$g(t_0) = (g_0g_1g_2g_3g_4 ...) = (1 0 0 1 1 ...),$$

where all bits in \underline{x} and \underline{g} are zero for x_{-i} and g_{-i} . Then the output (code) bit formed by the convolution of $x(t_0)$ with $g(t_0)$ is

$$\underline{y}(t_0) = \underline{x}(t_0) * \underline{g}(t_0) = 0.$$

For time $t_0 + \Delta t$, the sequences and output are

$$\underline{x}(t_0 + \Delta t) = (x_0 x_1 x_2 x_3 x_4 \dots) = (1 \ 0 \ 1 \ 1 \ 0 \dots),$$

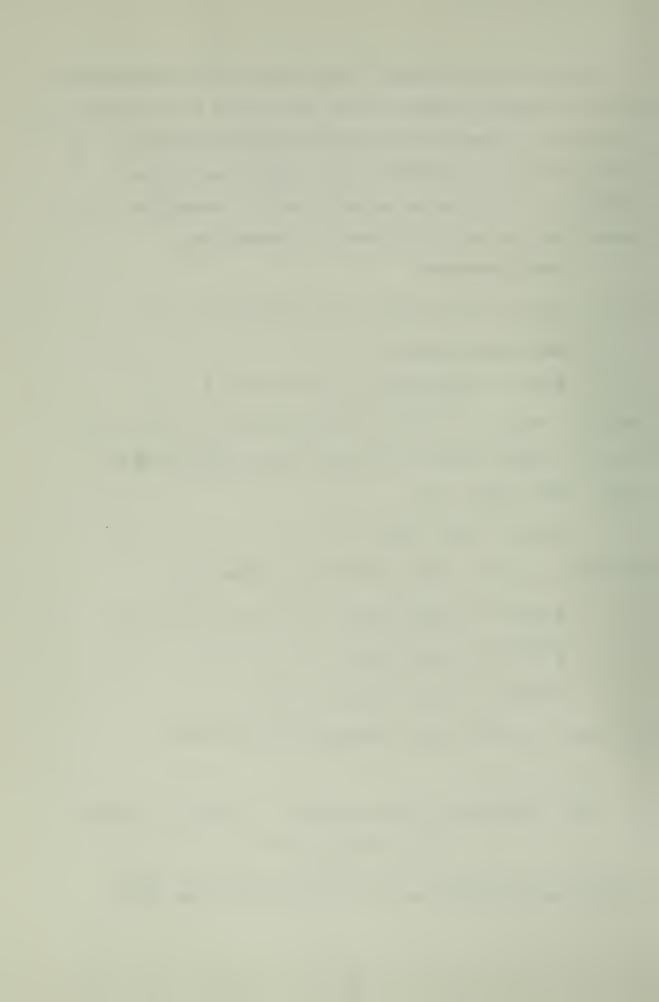
$$g(t_0 + \Delta t) = (g_0 g_1 g_2 g_3 g_4 \dots) = (1 \ 0 \ 0 \ 1 \ 1 \dots),$$

$$y(t_0 + \Delta t) = (x_0 \cdot g_0) = (1 \cdot 1) = 1$$
.

For time $t_0 + 2\Delta t$, the sequences and output are

The convolution of two functions, f_1 and f_2 , is equal to $\int_{-\infty}^{\infty} f_1(t-\tau) f_2(\tau) d\tau$,

which means one function is folded in time, then their product is integrated as one is shifted pass the other.



$$\underline{x}(t_0 + 2\Delta t) = (x_0 x_1 x_2 x_3 x_4 \dots) = (1 \ 0 \ 1 \ 1 \ 0 \dots),$$

$$\underline{g}(t_0 + 2\Delta t) = (g_0 g_1 g_2 g_3 g_4 \dots) = (1 \ 0 \ 0 \ 1 \ 1 \dots),$$

$$\underline{y}(t_0 + 2\Delta t) = (x_0 \cdot g_1) \bigoplus (x_1 \cdot g_0) = 0.$$

And the same procedure is applied to subsequent increments of Δt (one bit shift).

This technique extends the concept of block encoding to permit memory from bit to bit continuously as against memory within the block. Using the operation shown above, a conventional convolutional encoder (figure 2) may be defined as a linear sequential machine with k-inputs and n-outputs, where n > k, usually. This machine is constant, linear, causal, and finite state with operations over a finite field F, commonly binary.

The parameter k is the number of input bits which enter the encoder in a time increment (At). These bits along with others retained in the encoder memory (finite length), form n-output bits (code bits). For the remainder of this paper k will have a value of 1, but it should be remembered that this parameter can take on other values, as can be seen in figure 3.

The definition specified a finite state machine, whereas the example dealt with indefinite length sequences.

Since an infinite length memory is not practical it becomes
necessary to limit the basic concept (generator sequence)
and define some new expressions employed in the actual
encoder configuration.



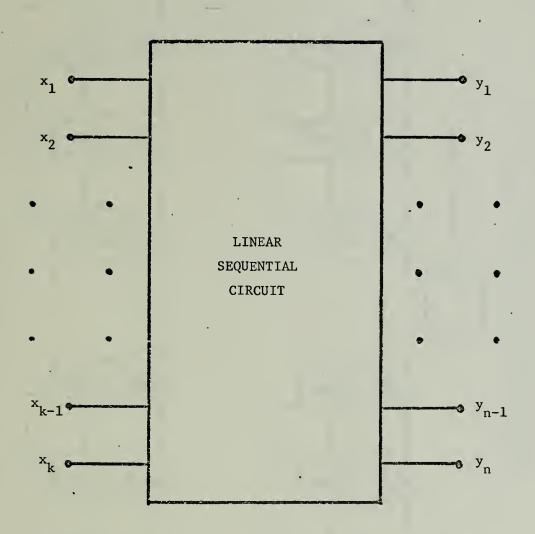
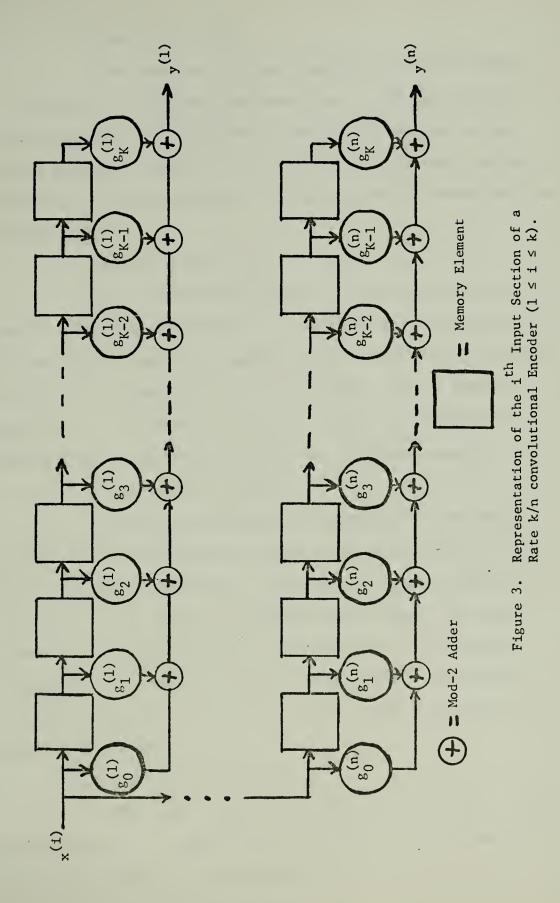
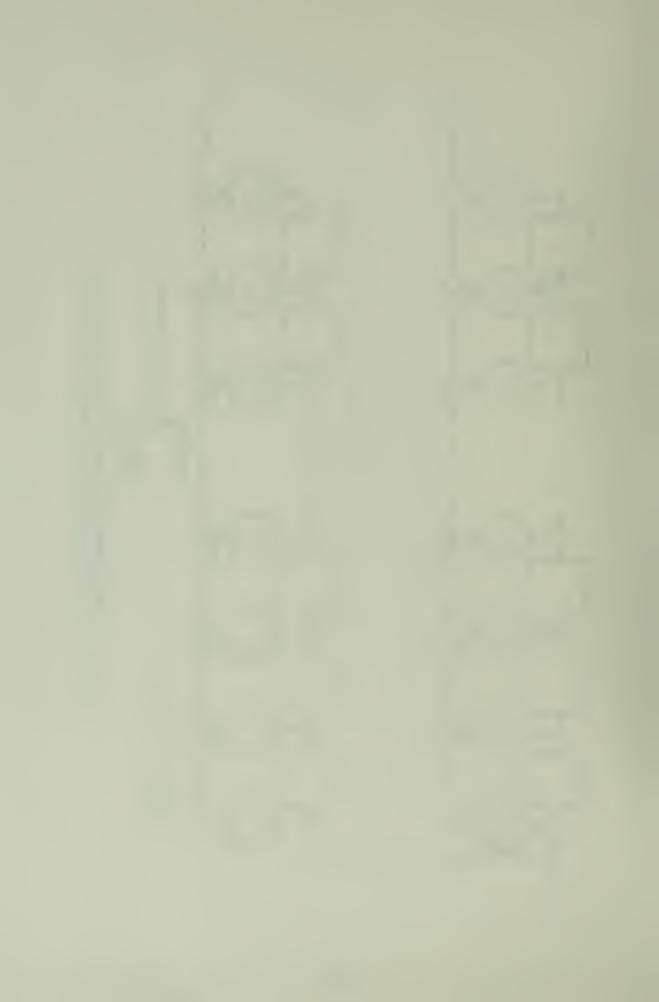


Figure 2. Conventional (n,k) Convolutional Encoder







a. Code Rate (k/n)

The code rate is an expression of the number of k-input (1) bits per n-output bits, that is, k/n (1/n). This value may be considered a very close approximation to the actual value. The actual value would also include a very small number of zero code bits used to terminate the code sequence.

b. Memory Length (M)

For a practical encoder <u>g</u> must be limited in length. The memory length is a measure of this length and is the minimum number of memory cells required to generate a code. A representation of an encoder, with a memory length of 2, is shown in figure 4. This configuration corresponds to the Mealy machine in automata theory.

c. Constraint Length (K)

A more conventional expression of the length of time which an input bit affects the output sequence is that of constraint length. This term is simply the memory length plus one, and is depicted as the number of memory elements in a Moore machine configuration of an encoder (figure 5). As may be expected this value is one factor in determining the complexity of the error detection and correction scheme.

d. Free Distance (d_f)

The term distance, as applied to coding, refers to the number of differing bits between two code sequences of the same length, as seen below:



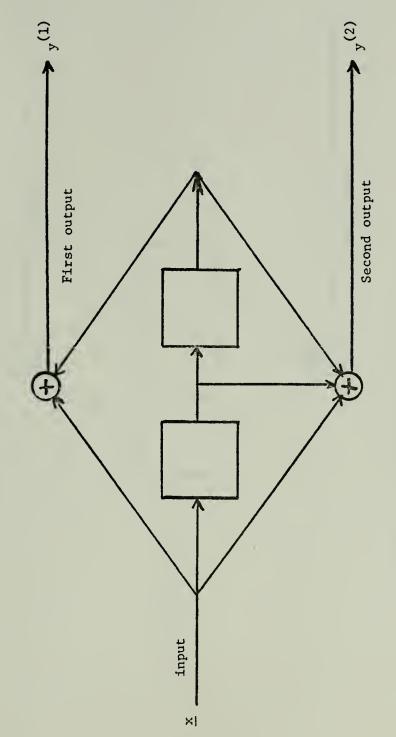


Figure 4. Mealy Configuration of a M = 2, n = 2, Binary Convolutional Encoder



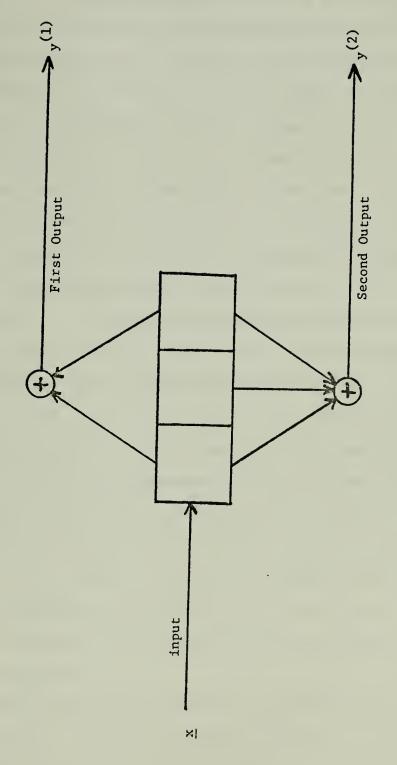


Figure 5. Moore Configuration of a K = 3, n = 2, Binary Convolutional Encoder.



code sequence 1: (1 0 0 1 0 1 1 0 0 1)

code sequence 2: (1 0 1 1 0 0 1 0 0 1)

Differences between the two sequences exist in the third and sixth bits only, therefore the distance between the two sequences is 2. When using block codes to construct a code sequence the minimum distance between all pairs of codewords (code blocks) is a definite indication of the error detecting and correcting capability of the code. However, if the code does not employ a block configuration, the use of this value may not be justified to indicate the codes error detecting and correcting capabilities.

This is the case when discussing convolutional codes. Free distance is the term for the value expressing the theoretical error correcting capability of a convolutional code. This value is defined as that minimum number of set bits occurring in a code sequence which resulted from the input of a nonzero sequence. Table I shows how the free distance (d_f) can be determined for a rate 1/2 convolutional code with K=3. As can be seen, the larger the value of K then the number of possible input sequence to be considered also increases at a great rate. But with the aid of computers the tedious grinding process is accomplished rather quickly.

The convolutional encoder is constructed to take full advantage of the free distance applied to a specific code rate and constraint length. This is accomplished through the proper selection of generator sequences. However, it



g	5	9	9	7	
X	11 01 11	11 10 10 11	11 01 00 01 11	11 10 01 10 1	and so on
×I	100	1100	10100	11100	

Minimum $d = d_{free} = 5$

Table I. Determination of free distance for Encoder in Figure 5.



should be noted that with the computers currently available the drudgery can be passed on to the machine.

2. Properties

The properties of the encoder, as related to the generator sequence, are discussed in this section. For convenience, the set of generator sequences (g_1, \ldots, g_n) used to generate the convolutional code is denoted by $[\underline{G}]$, a matrix representation of the encoder discussed in the next section. Figure 6 is useful in relating the following discussion to a physical communication system.

a. Property 1

Foremost, the useful encoder should generate a code which will yield the fewest number of errors in the codeword estimator. The estimator is a demodulation scheme at the receiver determining as accurately as possible the received sequence before actual decoding takes place. Along with this error minimization, the complexity of the estimator requires minimization to develop a useful error correction system. Error minimization and complexity minimization together may require some compromise in the practical system depending on the desired reception quality and system environment.

b. Property 2

The encoder [G] must have an inverse relation for decoding purposes. This is realized by the relation

$$\chi[\tilde{\underline{G}}]^{-1} = \chi[\underline{G}][\tilde{\underline{G}}]^{-1} = D^{p}\chi$$



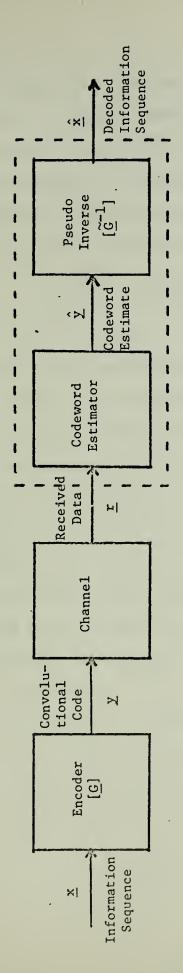


Figure 6. Block Diagram of Basic Communication System



for all \underline{x} . The matrix (decoder), $[\underline{\tilde{G}}]^{-1}$ is physically realizable and is a pseudo inverse, in that, the expression $[\underline{\tilde{G}}][\underline{\tilde{G}}]^{-1}$, yields a delay D^p , where p is the number of time intervals before decoding occurs in the expression. If p is zero the decoding occurs on receipt of the sequence and the above relation becomes

$$\chi[\underline{G}]^{-1} = \underline{x}[\underline{G}][\underline{G}]^{-1} = \underline{x},$$

where $\left[\underline{G}\right]^{-1} = \left[\underline{\tilde{G}}\right]^{-1}$ when p = 0.

A mention of the possibility of catastrophic error propagation, [Ref], is required at this time to stress the point that $[\tilde{\underline{G}}]^{-1}$ must be feedback-free. This may be interpreted as meaning that the n generator sequences, in polynomial form should not have a common factor. If a common factor exists then the input of a sequence with a finite number of set bits to the encoder, may be decoded, after noise is added, as a sequence with an infinite number of set bits. This is catastrophic error propagation and is avoided by making $[\underline{G}]$, thus $[\underline{\tilde{G}}]^{-1}$ feedback-free.

c. Property 3

The matrix $[\underline{G}]$ must also meet the requirements mentioned in the definition of a convolutional encoder.

(1) <u>Constant (time invariant)</u>. The time invariance of the encoder is represented by

$$[G](D^{p}x) = D^{p}y,$$



which means if all the inputs are shifted in time, then all the outputs are shifted accordingly.

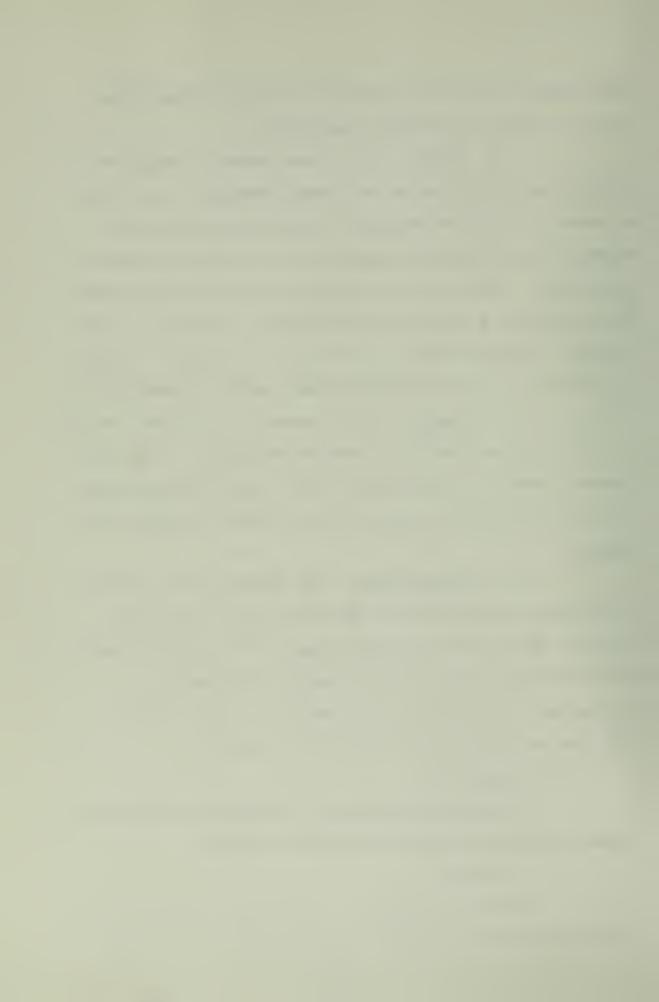
- (2) <u>Linear</u>. The output sequence resulting from the superposition of two input sequences, \underline{x} , must be equal to the superposition of the two output (code) sequences, \underline{y} , that would result from the inputs entered separately. This is also necessary for the multiplication of an input by a scalar as shown below. If $G:\underline{x}\to\underline{y}$, then $G(\underline{x}_1+\underline{x}_2)=G(\underline{x}_1)+G(\underline{x}_2)=\underline{y}_1+\underline{y}_2$, and $G(\alpha\underline{x}_1)=\alpha G(\underline{x}_1)=\alpha G(\underline{x}_1)$ where α is an element in the field F (usually GF(2)).
- (3) <u>Causal</u>. The existence of a nonzero output, y, prior to the input of a nonzero sequence, \underline{x} , is forbidden. This is accomplished by the encoder output being zero when its memory elements are all zero, therefore zero inputs.
- (4) Finite State. The states of the encoder are finite in number due to the value of the constraint length. Thus, a binary encoder has 2^{K-1} possible states. Each state being those input elements involved in the generation of the next output (code) bit, when combined with the next input bit entering the encoder.

d. Property 4

The chosen encoder $[\underline{G}]$ should have the minimum number of memory elements to generate the code.

e. Property 5

The chosen encoder $[\underline{G}]$ should generate a code yielding the fewest number of decoding errors per error



event (channel noise). Thereby, the fastest <u>correct</u> decoding decision is made at the receiver.

The preceding paragraphs provide a basis by which the acceptable class of encoders is greatly reduced in number. However, the selection of [G] in its optimum form for a given channel is a long drawn out process, possibly best suited for computer analysis. Theoretical selections have been made by many people, [Ref.], who based their decisions on the free distance alone.

3. Representation

The encoder configurations used to this point are accurate physical descriptions, but they lack a convenient form needed for analysis. There are five encoder representations which show varying degrees of the code's structure. Each is discussed in the following sections.

a. Polynomial

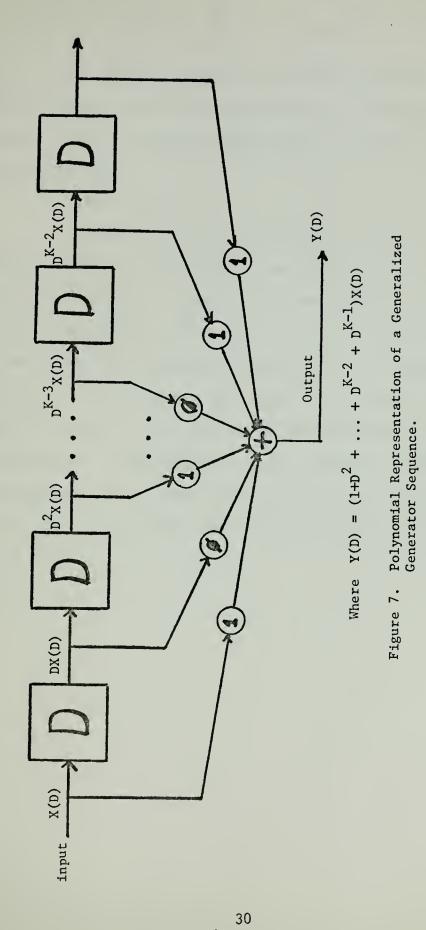
Using the D-transform, the input and output sequences appear as polynomials of degree much greater then the constraint length (K).

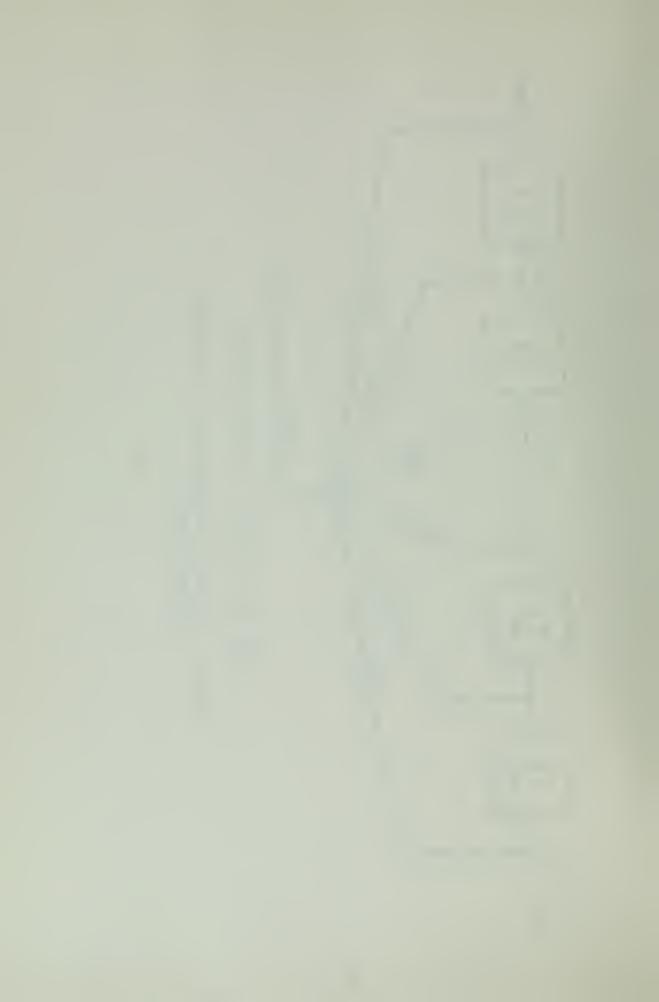
Input,
$$\underline{X}(D) = \dots + x_{-1}D^{-1} + x_0 + x_1D + x_2D^2 + \dots$$

Output, $\underline{Y}_{i}(D) = \dots + \underline{Y}_{i,-1}D^{-1} + \underline{Y}_{i,0} + \underline{Y}_{i,1}D$
 $+ \underline{Y}_{i,2}D^2 + \dots$

where $1 \le i \le n$. The generator sequence, for the Mealy machine configuration in figure 7, is a polynomial of degree equal to K-1. The mapping of $X \to Y_i$ is accomplished by polynomial multiplication.







$$\underline{Y}_{i}(D) = \sum_{j=0}^{L} (x_{j} \cdot g_{i,p-j}) D^{p},$$

where L is the bit length of the input sequence. This representation has little advantage in a code structure analysis, but it is very definitive as to the procedure for code generation.

b. Matrix

A matrix, $[\underline{G}]$ representation of a rate 1/n encoder starting at state zero and time zero is achieved by the manipulation of each generator sequence. When $\underline{y} = [\underline{G}] \underline{x}$, $[\underline{G}]$ may be shown as a matrix whose row vectors are the generator sequences (figure 8a). Using this notation restricts \underline{x} to be a length K. However, the requirement to change \underline{x} for each code computation is eliminated by the matrix in figure 8b. This notation incorporates the shifting of \underline{x} past each $\underline{g}_{\underline{i}}(1 \le \underline{i} \le n)$ into the matrix $[\underline{G}]$. For example, (figure 8 follows the example),



```
1001110011000...
                      K = 3
                     g_1 = (1 \ 0 \ 1)

g_2 = (1 \ 1 \ 1)
[\underline{G}] =
         11 01 11 00 00 .
          00 11 01 11 00
          00 00 11 01 11
          00 00 00 11 01
                         00 11
```



This form allows for a fast generation of the code and is definitely a model which could be implemented on a computer with little difficulty. Again, there is a lack of insight into the code structure except for the possible application of matrix algebra theory.

c. Tree

The most common representation is a tree diagram (figure 9) which incorporates the branch and nodal properties of the code generation. The base branch corresponds to the initial state of the encoder prior to a nonzero entry. The first node (a) is state zero for the encoder. When a 1 begins the sequence the first lower branch is chosen and the code is found on this branch leading to node (b) or state 1. The subsequent input bits dictate whether the tree is followed up or down,

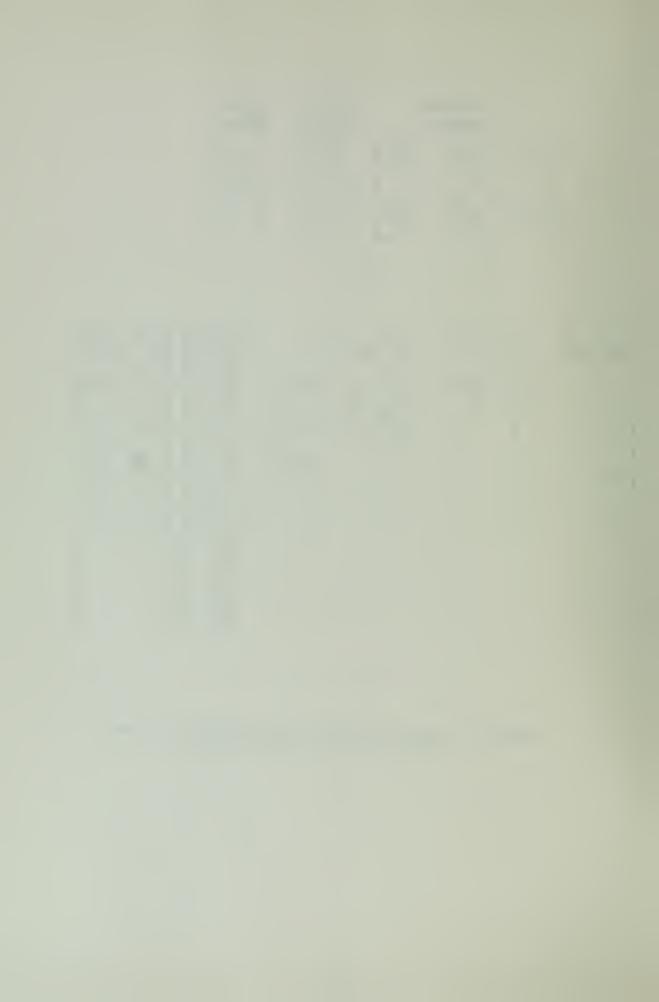


Encoder Matrix State Coutput
$$\begin{bmatrix} g_0^{(1)} & g_1^{(1)} & g_2^{(1)} \\ g_0^{(2)} & g_1^{(2)} & g_2^{(2)} \end{bmatrix} \cdot \begin{bmatrix} x_0 \\ x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} y_1^{(1)} \\ y_2^{(2)} \end{bmatrix}$$

(a)

(b)

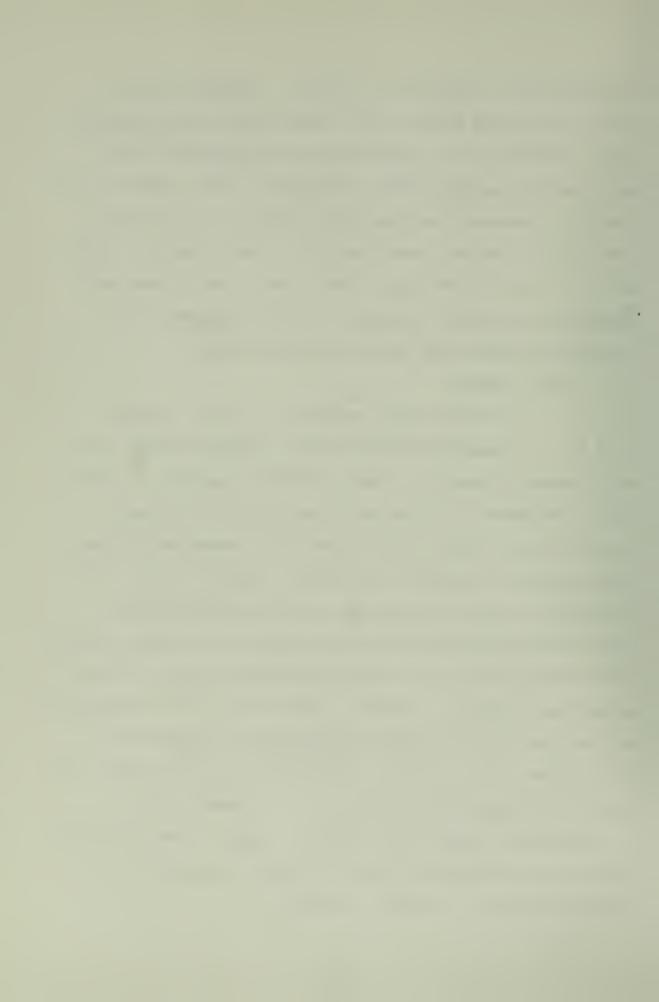
Figure 8. Generalized Matrix Representation of a Rate 1/2 Convolutional Encoder (K=3).



corresponding to inputs of 0 and 1 respectively. If this is continued to the Kth branch, all of the possible input sequences of K bits have been represented, thus each possible encoder state. Beyond the Kth branch it is readily recognized that the code symbols on the branches leaving from the two nodes labeled (a) are identical identical to those at the base of the tree. Even though the structure has become recurrent, for long sequences this diagram may become too large to analyze easily.

d. Trellis

Since the input sequence (1 0 0 ...) and (0 0 0 ...) generate the same n-bit codewords after the third branch (figure 9), then both nodes labeled a can be joined together. The recursive character of the tree diagram lends itself to be redrawn with remerging branches, thus forming a trellis (criss-cross) diagram (figure 10). The encoder state is the basis for the trellis diagram. These states represent those input bits in the memory cells which will generate the code bits when the next input bit enters the encoder. Therefore, there are 2^{K-1} states on either side of the diagram representing the present and next states. The branches connecting the states denote the code bits being generated when a l (dashed line) or a (solid line) enters the encoder. Again, after the third input bit the complete trellis diagram is specified and is repeated for all succeeding branches.



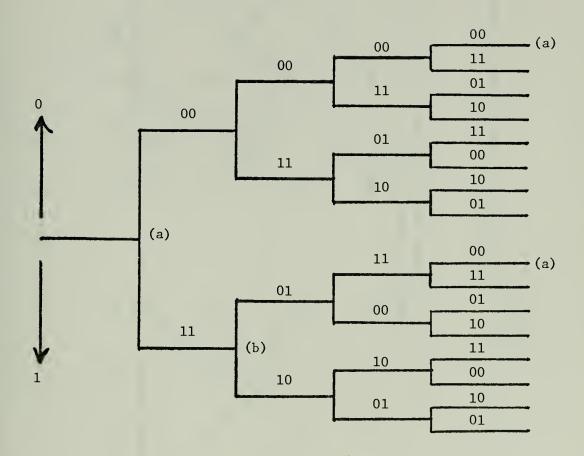


Figure 9. Tree Representation of Convolutional Encoder in Figure 5.



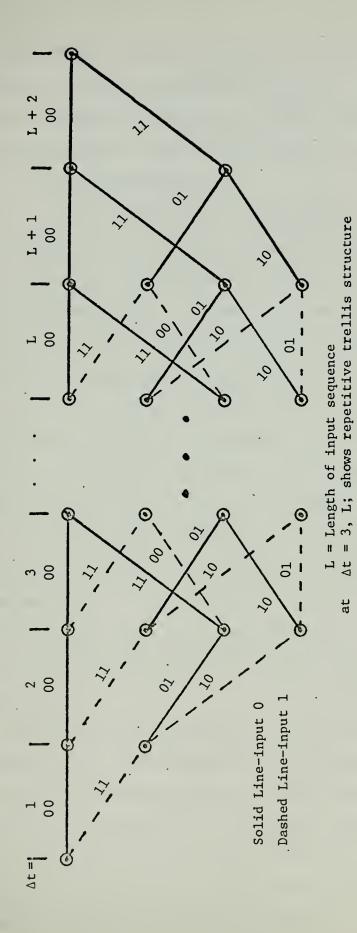


Figure 10. Trellis Representation of Convolutional Encoder in Figure 5.



For short constraint lengths (K < 10), this representation is highly desirable due to its compactness. The trellis diagram is used in the Viterbi decoding algorithm and easily lends itself to be listed in a computer program.

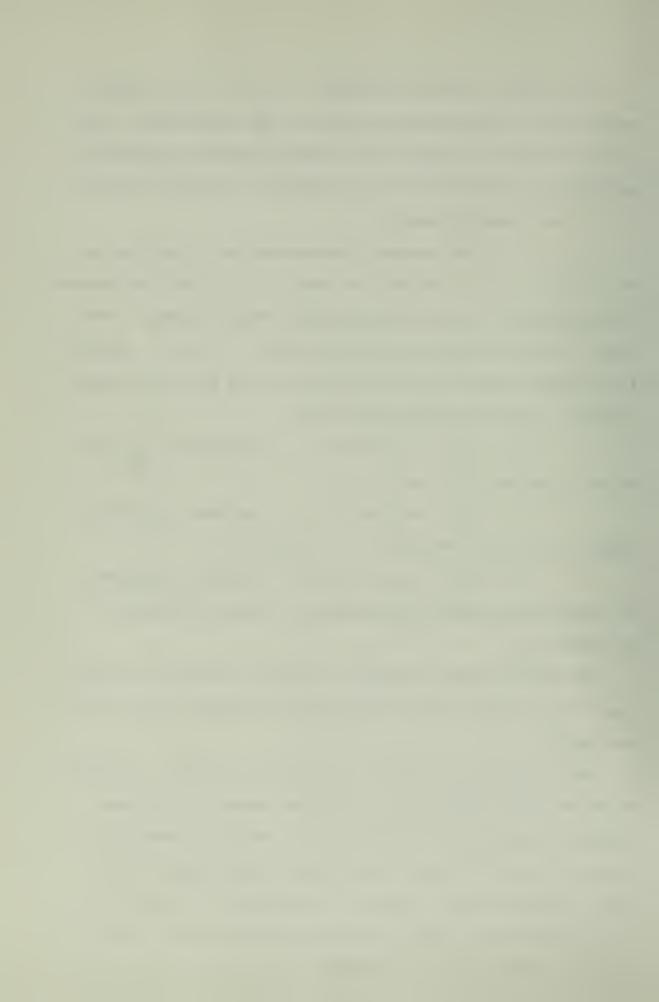
e. State Diagram

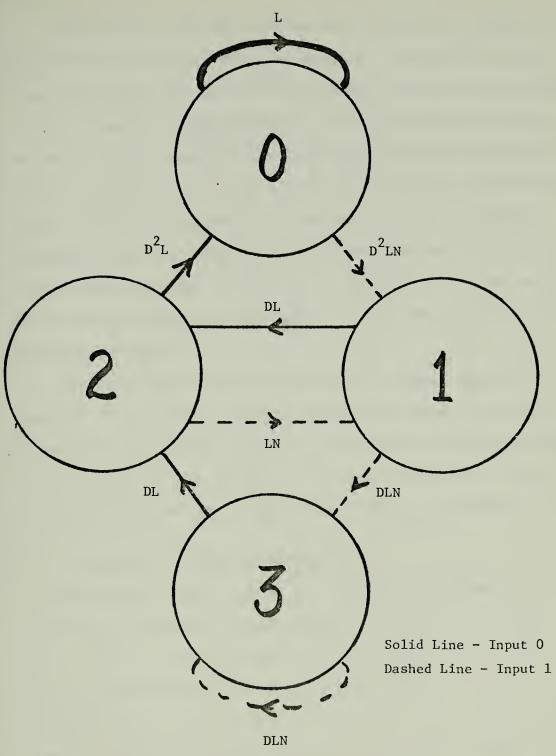
The last encoder representation is similar to the trellis, but is spread out more to allow more parameters to be placed on the branches between states (nodes). The state diagram (figure 11) has the input 0 and 1 denoted in the same manner as for the trellis, but some additional notation is placed on the branches.

- (1) \underline{D}^{q} . The value of q denotes the weight of the code bits for that branch.
- (2) \underline{L}^r . The value of r denotes the branch length of a path from state x to state y.
- (3) \underline{N}^{S} . The value of s denotes the number of input one branches encountered in a path from state x to state y.

All of the above notation is used in figure 11 and the results of a state path for the input sequence (1 0 1 0 0) are shown.

Since the state diagram is a directed graph, a transfer function can be determined using the theory of directed graphs, [Ref. 4, pp 2A-1-2A-11]. The transfer function consists of various powers of the three measurements listed above. These values are used to determine the properties (D, L, N) for all paths in the convolutional code, when the transfer function is in expanded form.





 \underline{X} = (10100); Path Parameters = $D^6L^5N^2$

Figure 11. State Diagram Representation of Convolutional Encoder in Figure 5.



The trellis and state diagrams are the most complete representations and offer the analyst a chance to study the path structure of the convolutional code. Each diagram yield a compact representation, easily arranged for small values of K. However, the looping branches necessary for the construction of a state diagram become very confusing and difficult to arrange for larger constraint lengths.

Therefore, the trellis diagram is not only easy to construct and understand, but if the values of D, L, N, are needed for analysis they can incorporated into the diagram in an orderly fashion.

The discussion of convolutional encoding principles was basic and is by no means a complete detailed course in convolutional codes. However, the purpose of this section is to introduce the reader to concepts which will aid him in his understanding of the thesis computer program.

B. PRINCIPLES OF VITERBI DECODING

Decoding is the inverse operation to encoding and is intended to recover the source bits with all, or almost all, of the channel errors removed. The decoder, which may be implemented as hardware or software, utilizes the encoded bits to detect and/or correct errors. Error detection is similar in complexity to the encoding operation. Error correction, however, is inevitably a more complicated process than encoding, since the goal is to reduce the probability of a decoded bit error.



A scheme for decoding convolutional codes was proposed by Viterbi in 1967, [Ref. 8]. It was shown by Viterbi that an optimum decoding procedure existed for a statistically independent (bit to bit) input sequence transmitted over a channel whose errors occur independently from channel bit to channel bit. Subsequently, Forney found that the Viterbi decoding algorithm is synonomous with maximum likelihood sequence decoding, [Ref. 3].

1. Description

Simply stated, the Viterbi algorithm is a solution to the problem of finding the most likely encoded sequence through a state (finite) diagram representing the encoder. For a decoder to minimize the overall error probability of a decoded bit by brute force, maximum likelihood decoding would mean calculating the likelihood of the received sequence on all paths of the encoder state diagram. However, there are two factors which reduce the complexity of this problem. The first is the fixed periodic structure of the encoder trellis diagram, and the second is the code characteristic of remerging paths after the same K input bits are applied to two different paths (figure 12). For these reasons, the trellis diagram is an ideal tabular representation of the flow of the code at any instant.

The decoding process, as mentioned above, was found optimal for a statistically independent input sequence in discrete time. Along with this stipulation, the channel noise is also memoryless, as is the case for a binary



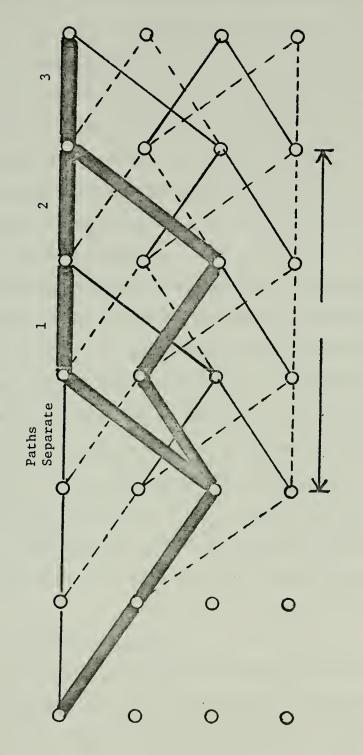
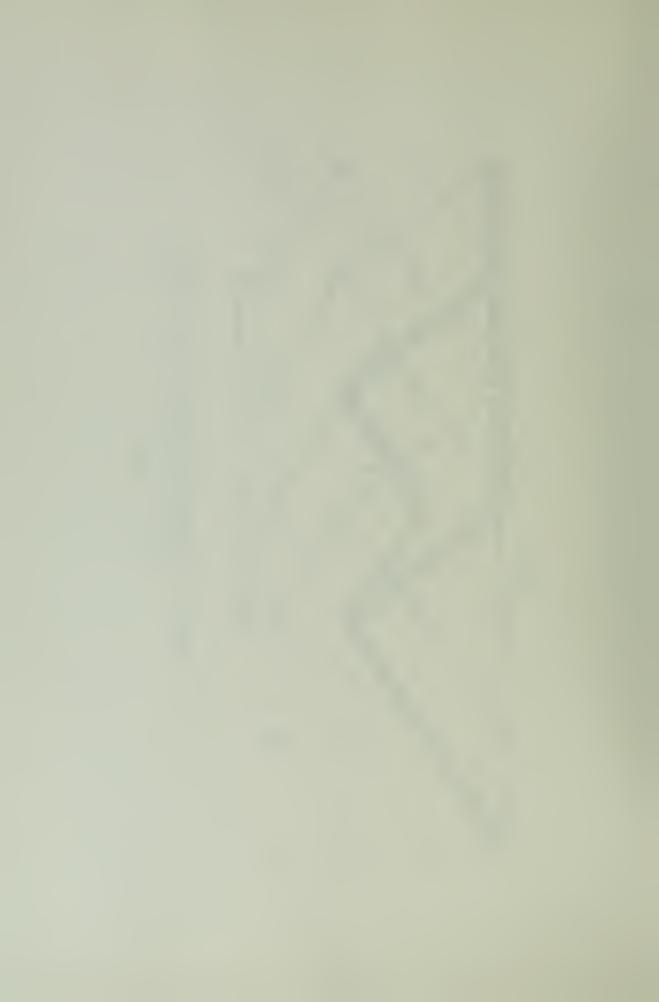


Figure 12. An Example of Remerging Path in Trellis Diagram of Convolutional Encoder (K=3).



symmetric channel (BSC) with hard decision demodulation (2^{1} levels) or an additive white gaussian noise (AWGN) channel with soft decision demodulation (2^{Q} levels, Q > 1). The BSC errors transform a 0 to a 1 and a 1 to a 0 and occur independently from bit to bit with probability p. In the AWGN channel, the probability of a given quantized value (0 to 2^{Q} -1) of a received bit is determined from the gaussian probability density function. These values of the received bits are used to determine the most likely received sequence.

A scoring procedure is employed indicating the trellis path which shows the least difference from the received sequence. This is accomplished by using the concept of distance for the BSC and a numerical difference for the AWGN channel. The latter may be called the innerproduct of the received bit and the calculated (trellis) transmitted bit. This is implemented digitally by taking the exclusive OR of the two Q bit representation of the bits above. Both (BSC and AWGN) techniques yield a value that can be used to determine the most likely (lowest score) path.

2. Implementation

In order to describe effectively the implementation of the Viterbi decoding algorithm an example follows with step by step explanations supplemented by appropriate diagrams. This example will be for a rate 1/2 convolutional code with K=3. The generator sequences are $5_8(1\ 0\ 1)$



and 7₈ (1 1 1). The following sequence is the encoder input: (1 0 1 1 0 0 0 1 1 0 1 0 0 0 1 0 ...).

The following subsections are the steps of the Viterbi algorithm decoding the perturbed (received) sequence.

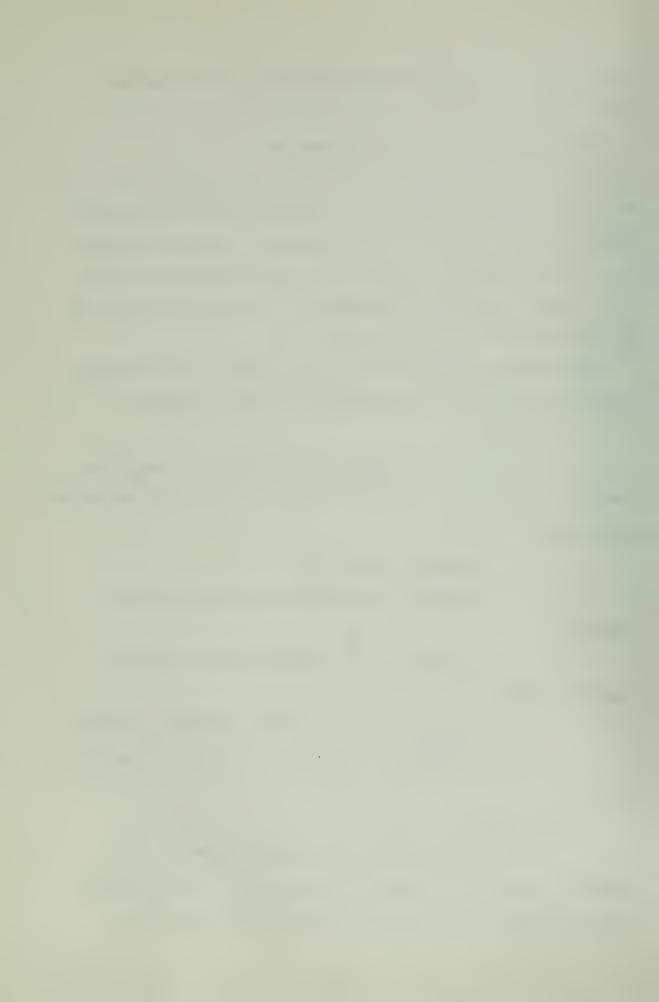
a. Step 1

The following figure and tables are set up to indicate the trellis structure, the path (survivor) sequences and the path scores.

- (1) Trellis. (Figure 10).
- (2) <u>SSEQ(I)</u>. The present state survivor sequence.
- (3) <u>SCORE(I)</u>. The present state survivor sequence score.
 - (4) SSEQ(J). The next state survivor sequence.
- (5) SCORE(J). The next state survivor sequence score.

b. Step 2

An initialization of tables (2) and (3) is shown in figure 13. Tables (4) and (5) are not considered until the first group of 2(n) received bits enter the



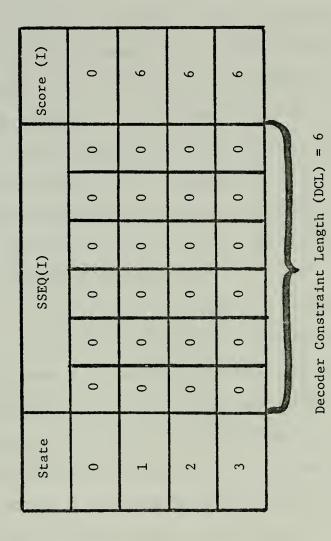


Figure 13. Present State Initialization for Viterbi Decoding Algorithm.



decoder. The all zero sequences placed in SSEQ(I) depicts the assumption that the encoder had no set bits entered prior to the beginning of the message under consideration. A decoder parameter is the length of the survivor sequences used to hold path estimates until a bit is decoded with the desired probability of error. This length is called the decoder constraint length (DCL), whose value is 6(2 x K) for this example. Also initialized is SCORE(I) so that a score of zero is in state 0 to denote that the encoder is assumed to have started from this state. The other states are assigned scores which demonstrate the unlikelihood of the encoder starting from these. Normally, a value of 2 x K is sufficient, which is 6 in this example.

c. Step 3 (Figure 14)

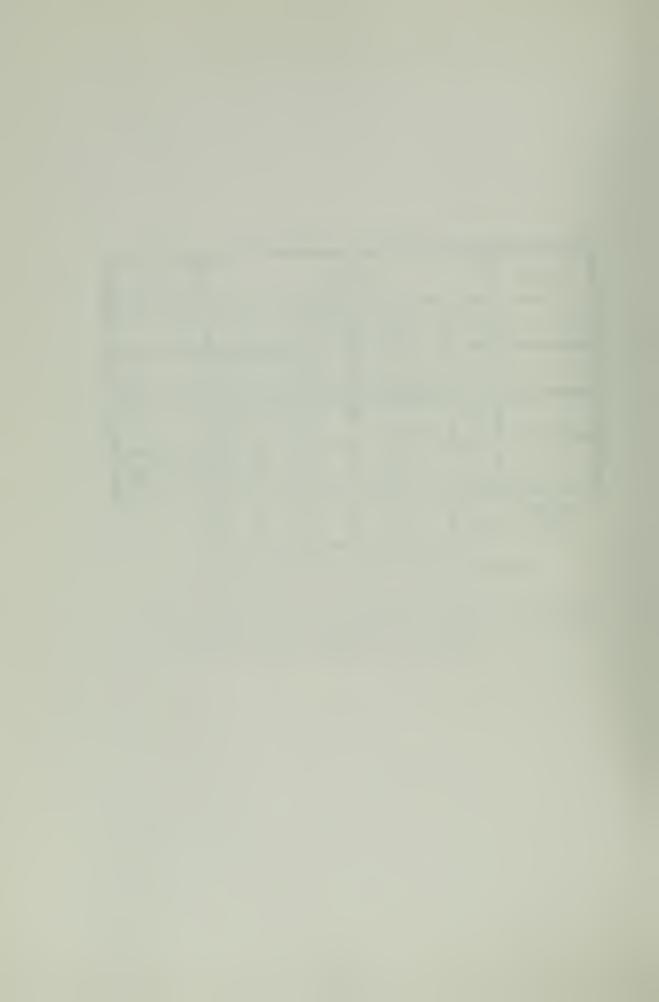
This step is the first in the actual decoding process. However, it will become obvious that it is recursive throughout the remainder of the algorithm. Now, the first 2 received bits (10) enter the decoder. These bits are compared with each pair of code bits on the branches of the trellis and a distance (Δ) is determined for each branch. This Δ is then added to the present score of the corresponding present state. Now there are two scores coming in on the branches to each next state. At this time, a decision is made as to which branch, coming into each next state, has the lowest score. If the scores are identical then an arbitrary choice can be made, decode estimate is zero for this example or an alternative may be exercised to



	State			SSE	Q(J)			Score (J)
	0	0	0	0	0	0	0	1
	1	0	0	0	0	0	0	1
	2	1	0	0	0	0	0	6
	3	0	0	0	0	0	0	6
•	Decoder Input	10						

Present State Decoded Bit = 0 From State 0

Figure 14. Next State Tables at the Completion of the First Shift of 2-Bits Into the Decoder.



further evaluate the Δ added to the score in SCORE(I). When all the next states have a score, they are entered in SCORE(J). Then the next state's survivor sequences are determined for entry into SSEQ(J). This is accomplished by determining what bit, 0 or 1 was dropped from the present state at the end of the minimum score branch for each next state. Then, this bit is shifted into the beginning of the appropriate present state sequence (SSEQ(I)) and the entire sequence is then placed in the SSEQ(J) table, corresponding to its next state.

The oldest bit just shifted out of the sequence in SSEQ(I) at state 0 is the most likely decoded bit since it is associated with the minimum score (0) sequence in the present state. The bit decoding, after a length of DCL, minimizes the effect of randomly spread errors in the received sequence. Again, if the scores of two or more sequences are equal, then a decision is made according to a more detailed comparison of the scores in SCORE(I).

d. Subsequent Steps

Since the most recent paths and scores are now in SSEQ(J) and SCORE(J), the roles of present and next are swapped, $(I) \leftrightarrow (J)$, and step 3 is carried out again. Thus, after each decoding bit decision, the (I) and (J) are swapped, and step 3 is repeated time and again. Figure 15 shows the decoding steps for four more shifts of the decoder input. The tables, after the eighteenth shift, are shown in figure 16.



Score(J

SSEO(J)

State

2nd

0000

0000

0000

0000

0 0

0

7

000

0

0

Decoder

Input

 \sim

3rd

			I					
	State		S	SEC	SSEQ(J)			Scor
	0	0	0	0	0	0	0	2
	1	1	0	0	0	0	0	1
	2	0	0	0	0	0	0	3
_	3	0	0	0	0	0	0	3
	Decoder	00	0001	10				
_	Input							

5th

Score(J)

SSEQ(J)

State

4th

0000

000

0000

0

0 0

00

0

00

0

0

00

2

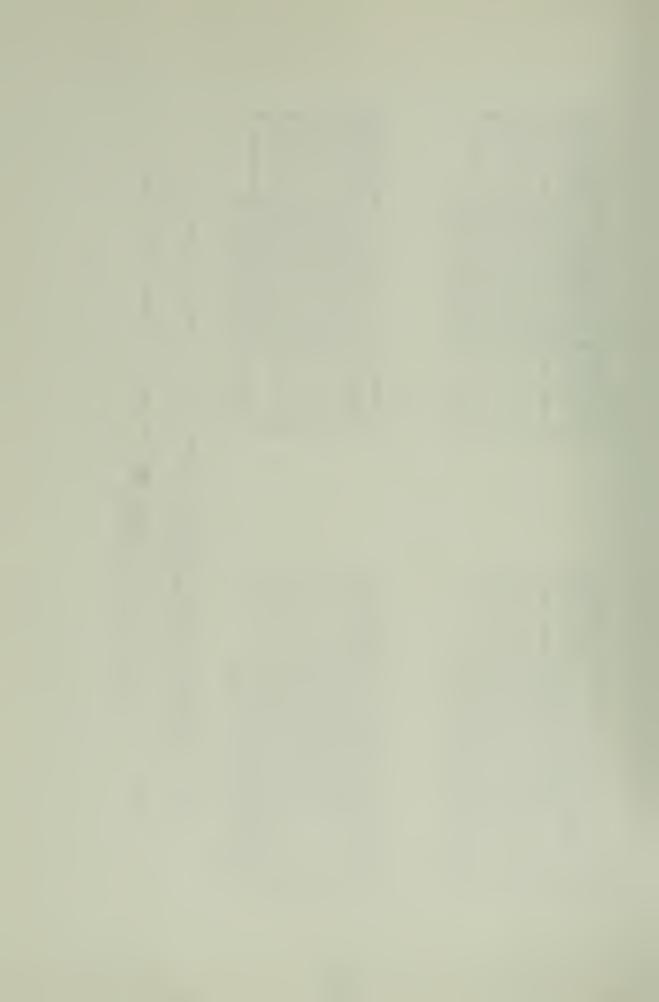
Decoder

Input

State		S	SEQ(J	رح)			Score(J)
0	τ	0	1	0	0	0	3
1	0	0	0	0	0	0	3
2	1	0	7	0	0	0	2
3	7	0	7	0	0	0	2
Decoder	11	10	00	01	10		

The present state tables for each shift are derived from the previous next state tables. Note:

The Next State Tables for the Second Through Fifth 2-Bit Shift into the Decoder. 15. Figure



Score (J)	4	5	9	9		
	1	1	1	1	11	
	0	0	0	0	00	
SSEQ(J)	0	0	0	0	11	
	0	0	0	0	11	
	1	1	1	1	11	
	0	1	1	1	00	
State	0	1	2	3		

Decoded Bit-Bold Outline

Decoded Output = $(1 \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 1 \ 0)$

The Next State Table after 18 Shifts and the Decoded Output to that Point. Figure 16.



It is noticed, at this time, that the first 8

(DCL + K-1) bits are zero. This is explained by the presense of 6(DCL) zeroes in the initial SSEQ(I) and the 2(K-1) zeroes in the encoder when the first nonzero code bits were generated.

Another note should be made of the ease with which a soft decision demodulation scheme could be incorporated into the scoring process. This dimension would produce a more accurate representation of the likelihood of a sequence and possibly eliminate the need for arbitrary decisions, which may also be time-consuming.

At a first glance this procedure may seem strange or awkward, but there can be no doubt that the Viterbi algorithm is easily computer (hardware or software) implementable. The recursive nature of the primary decoding step is the prime factor in controlling the size of that implementation.



III. COMPUTER PROGRAM

The term simulation in the title of this thesis should not be construed to mean the encoder and decoder operations (Programs) are simulated. By no means is this the case, for the rate 1/n convolutional encoder and the Viterbi decoder are software implementations that could be used in an actual system. Of course, some form of synchronization is needed for practical operation, but in this program that is assumed to have been accomplished by elements (hardware or software) preceding the decoder in the receiver.

A. CHANNEL NOISE

Actually, the simulation occurs when a channel is described in the program by a noise generating section. This section includes a quantization segment, random number segment, noise generation segment, and perturbation (summing) segment. The following paragraphs are discussions of these four divisions of the channel noise program.

1. Quantization

This part of the program uses the encoded sequence as an input, then passes this sequence on to the noise sections after Q zeroes or ones have been substituted for each 0 or 1. When Q=l is a program input this segment is bypassed for apparent reasons.

2. Random Numbers

The random numbers generated in this program were obtained by using the Lehmer congruential method.



$$X_{n+1} = aX_n + b \pmod{T_0},$$

where a = 257, b = 1, and $T_0 = 2^{16}$. The term X_0 , starting number, is varied to provide representative sequences of the distribution shown in figure 18. These numbers are used to determine the time between set bits in noise sequence. The period of the random number sequence is 2^{T_0} , therefore, a large sampling of the sequence approaching 2^{T_0} would result in a binomial distribution. However, the test runs used to determine results in this thesis employed message inputs of 10,000 bits in length. Thus, the distribution (dots) shown in figure 17 is a better representation of the time between set bits in the noise sequence.

3. Noise Generation

After a random sequence has been generated in the previous segment, 2., a noise sequence is formed using the numbers. Multiplication of the number of set bits in 16 bits (T), the length of one random number, with powers of $2(2^{-2},2^{-1},2^0,2^1)$ determine how many zeroes will occur before the next set bit in the noise sequence. For example, if the random number being considered by the program is 0110011100100100, then its weight is 7_8 or 111_2 . If the noise parameters (core locations 10230 and 10236) specify multiply by 2^{-1} , then the number 7_8 is shifted one place right and becomes 3_8 . Likewise, if multiply by 2^1 is entered, then 7_8 becomes 16_8 . These new numbers are then used to determine the space between set bits in the noise sequence. Each 16-bit number from the congruential random



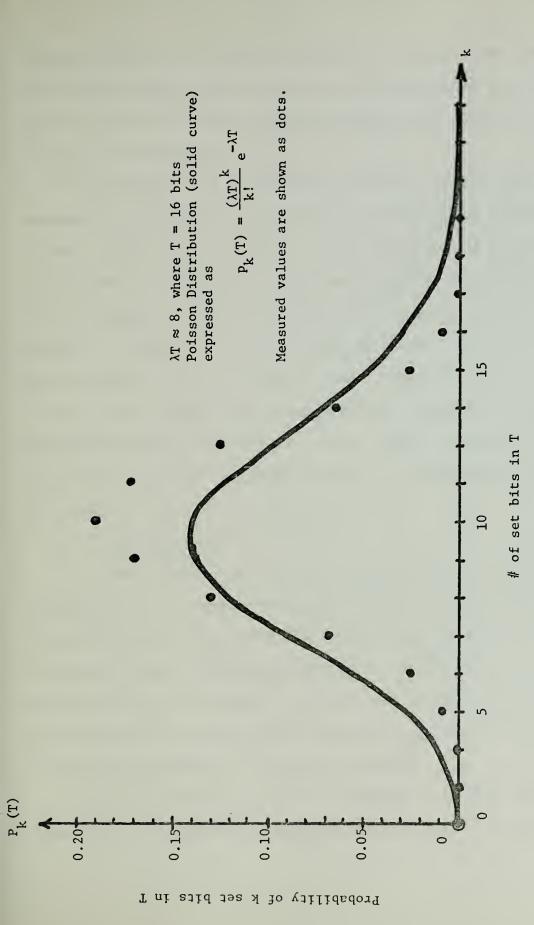


Figure 17. Comparison of Congruential Random Number Generator (10^5 bits) with Poisson Distribution.



number generator is used to generate a space. The number of 16-bit numbers used in one run is determined by the number of code bits which are present when the noise is added to the code sequence.

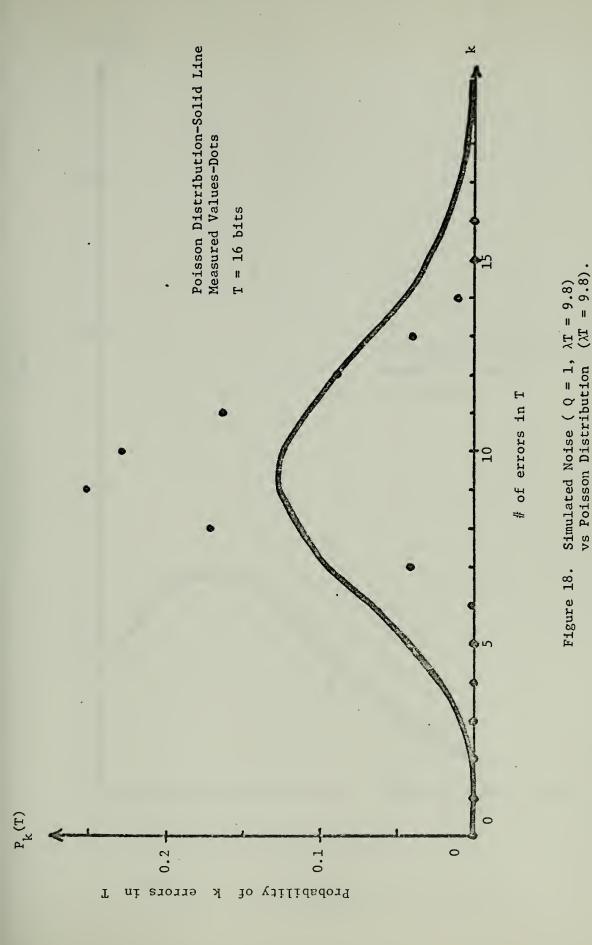
The variation in the set bit density for the noise sequence is analogous to varying the density of channel errors. This fact is used in the evaluation of the codes in section IV. Figures 18 through 23 show the probability of k errors in 16 channel bits (Q = 1, 2, 3) versus the number of errors, k, in 16 channel bits. The plots are for averages (λT) of about 10 and 2 errors per 16 channel bits. Also shown is the corresponding plot of the Poisson distribution as a continuous curve. Any discrepancy between the theoretical and measured (dots) is attributed to the 16 bit length constriction primarily.

4. Perturbation

The purpose of this last segment of the noise simulation is to simply exclusive OR (additive noise) the noise sequence to the quantized encoded sequence. This operation forms a perturbed sequence, which is the received sequence for the decoder. If this was to be changed to multiplication or some other operation another noise form could be simulated for the coding scheme.

All of the details, as to programming specifics, are discussed in Appendix B, along with a program listing.







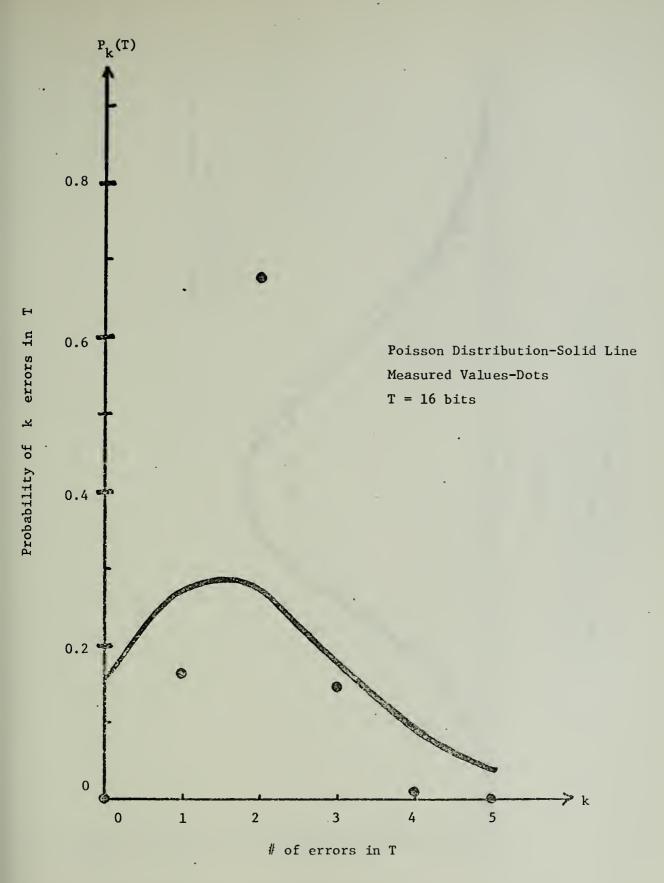
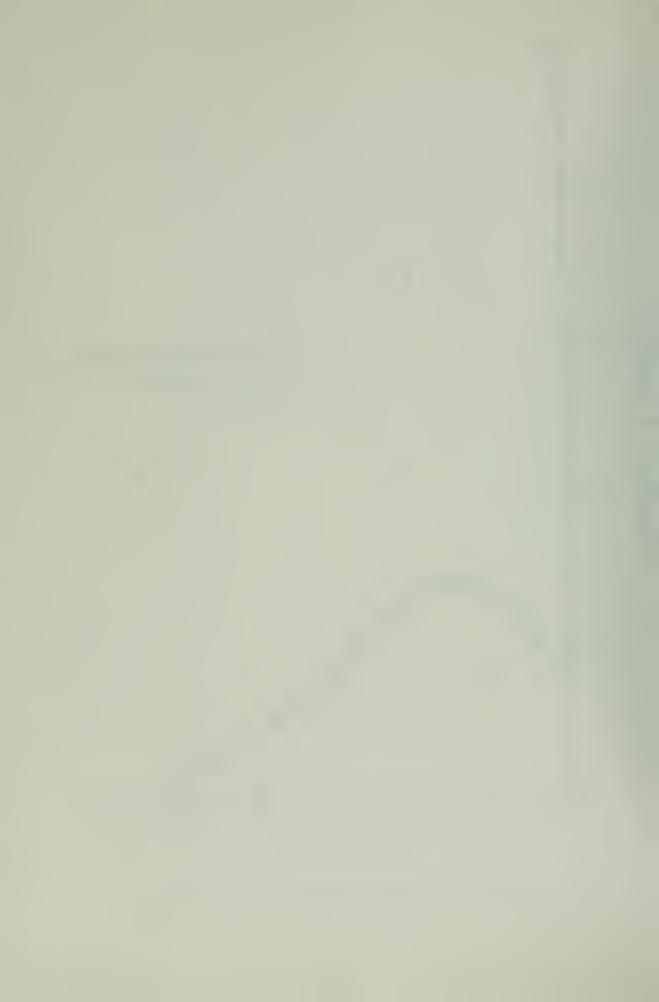
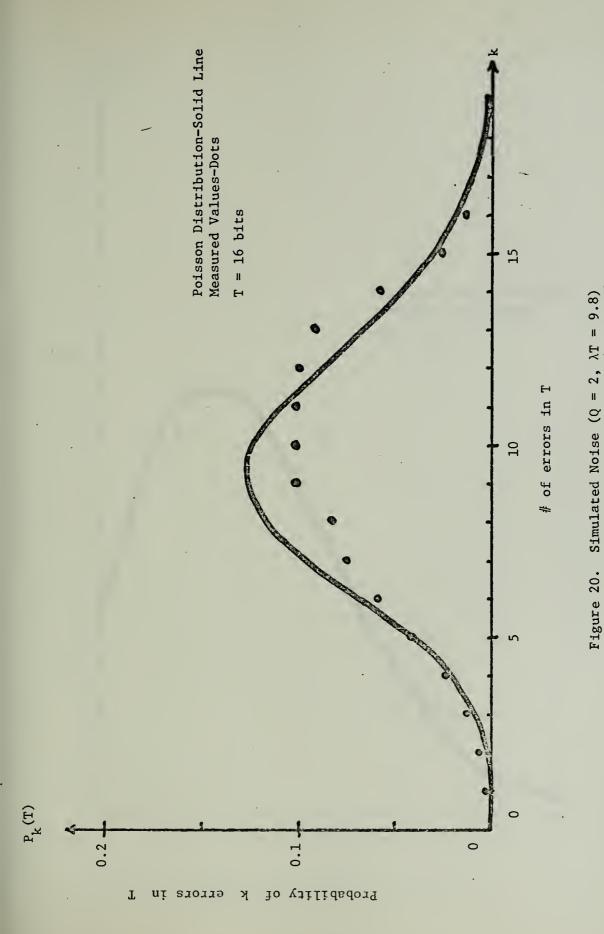


Figure 19. Simulated Noise (Q = 1, λT = 2.0) vs Poisson Distribution (λT = 2.0)





vs Poisson Distribution ($\lambda T = 9.8$).

58



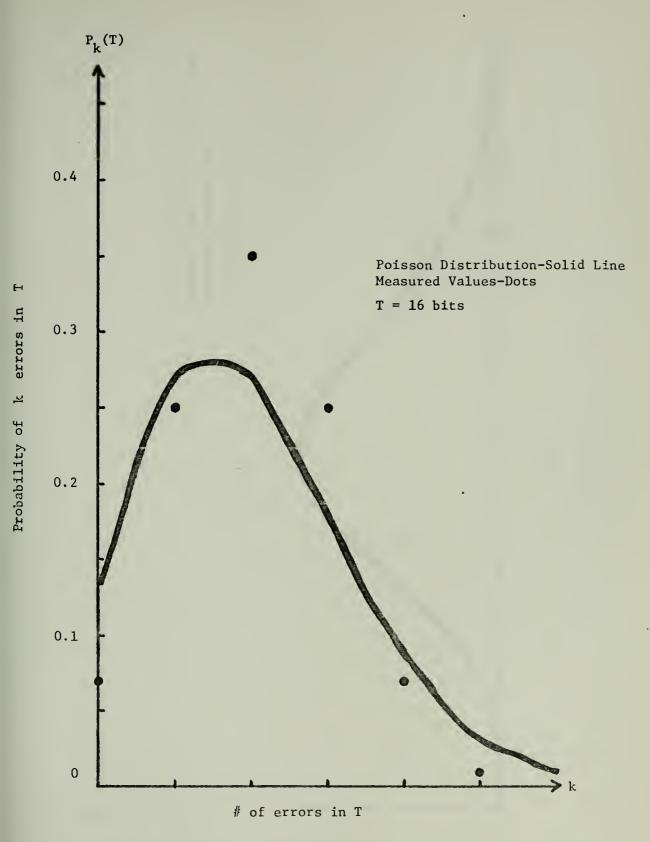
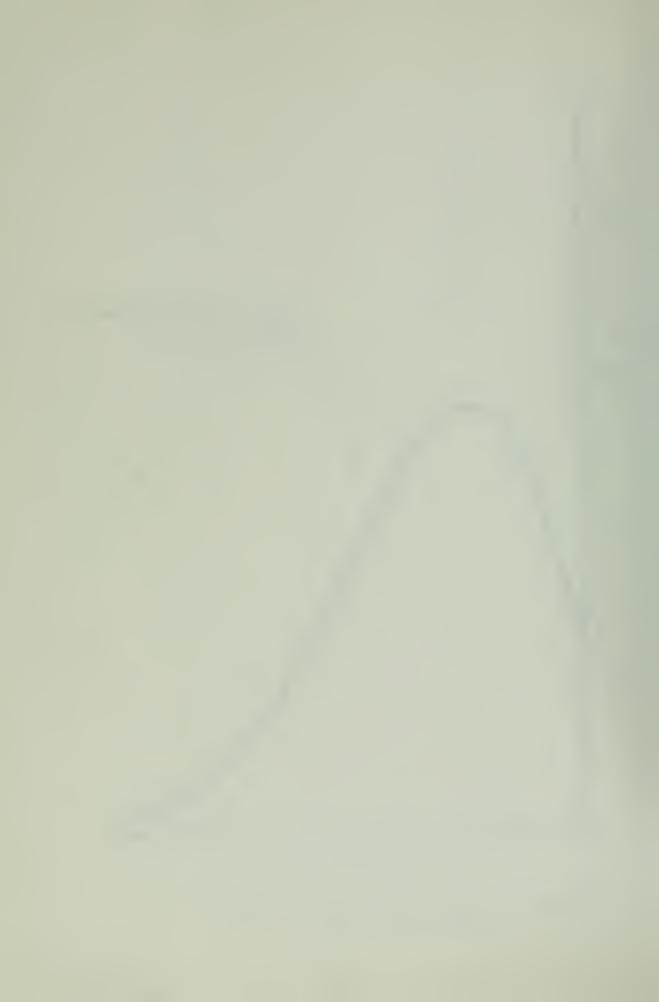
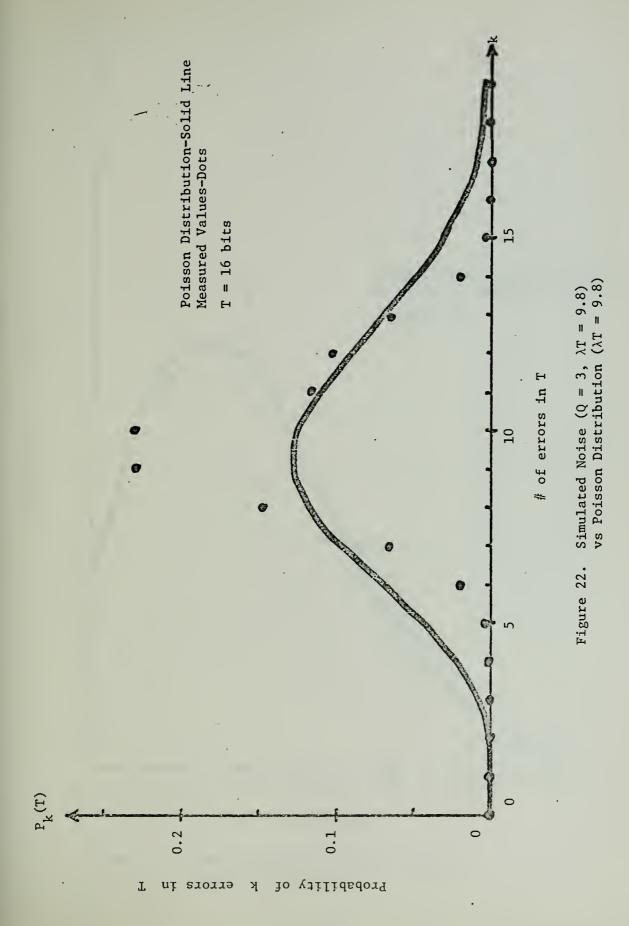


Figure 21. Simulated Noise (Q = 2, λT = 2.0) vs Poisson Distribution (λT = 2.0)







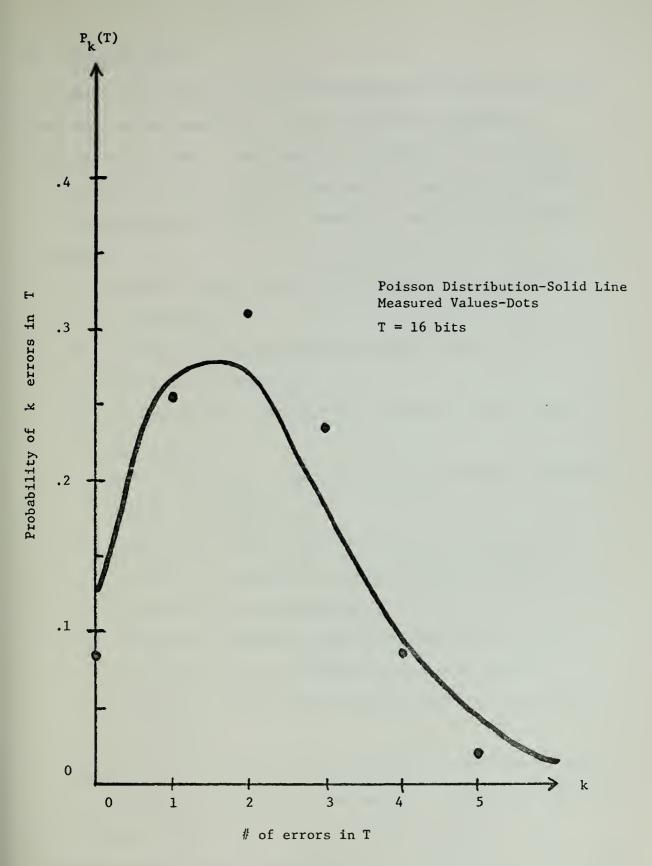
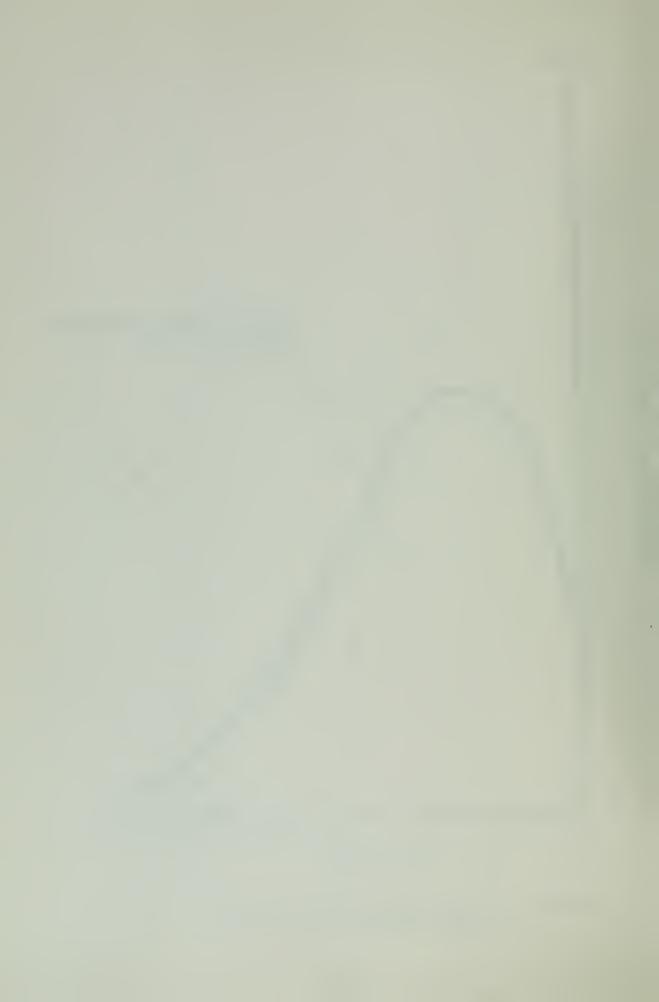


Figure 23. Simulated Noise (Q = 3, λT = 2.1) vs Poisson Distribution (λT = 2.1).



B. PROGRAM FLOW

The four major sections of the program are the encoder, decoder, noise generator, and the message generator (ASCII 7-bit code). An appendix is devoted to a detailed listing and brief discussion of each of the above sections.

The parameters that are needed to initiate the simulation are:

- 1. N; the inverse rate $(1/N^{-1})$ (memory location 10200 in Appendix F).
- 2. K; the encoder constraint length (memory location 10206 in Appendix F0.
- 3. Q; the quantization levels (memory location 10214 in Appendix F).
- 4. DCL; the decoder constraint length (memory location 10222 in Appendix F).
- 5. Noise parameters; operation (∴/x) and operand (1,2,3,...) (memory locations 10236 and 10230 respectively in Appendix F).
- 6. Generator sequences; representations entered so that first cell in encoder is bit 0 (memory locations 13760-13776, where G₁(13760, G₂(13762,..., G₈(13776)).

Another programming concept, position independent code (PIC), is used to allow the user to move the entire program or any part (with few changes) to another part of core.

This approach introduced the need for a program segment that initializes all addresses and counters (constants) used in

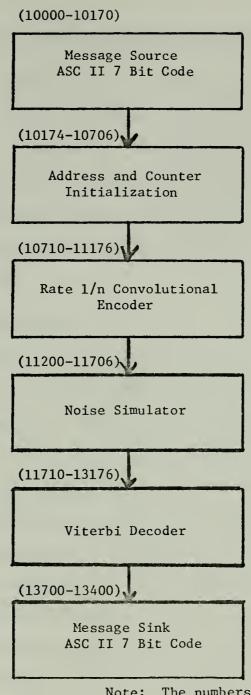


the program. The listing and a brief description of this segment are included in Appendix D.

The entire program, in block form, is depicted in figure 24. If the reader is interested in a detailed program description he is referred to Appendices B-E.

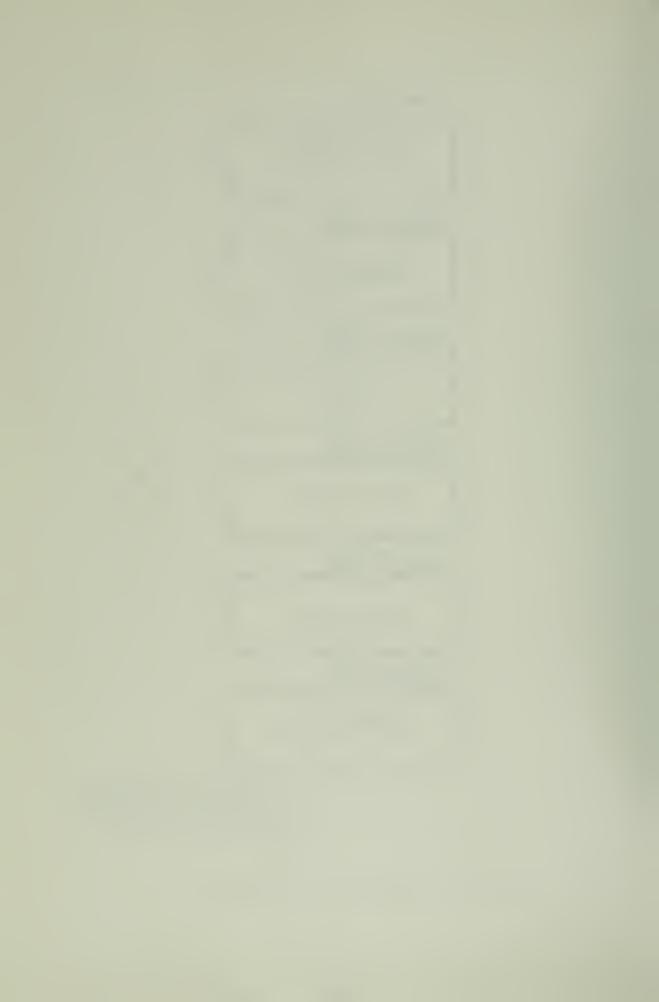
Appendix A contains a map of that part of core used for the implementation of the position independent code.





Note: The numbers in parentheses are actual addresses occupied by the instructions corresponding to a particular flow chart block.

Figure 24. Block Diagram of Program Flow.



IV. RESULTS AND CONCLUSIONS

The term best code is used in many papers, but for the most part the use of the term best code is not defined in sufficient detail. This is one descrepancy that will be avoided by this thesis. Included in this section is a summary of the computer results obtained from a best code (defined below) determination procedure and encoder/decoder parameter variations.

A. BEST CODE DETERMINATION

The determination of a best code for a specific channel a simulated channel in this paper, follows a procedure based on Shannon's fundamental theorem for a discrete channel with noise. This procedure is best described using Shannon's representation of the attainable region in a graph (figure 25) of H(x) (information rate) versus $H_{y}(x)$ (probability of decoded messager error). If $H(x) \leq C$ (channel capacity), then Shannon shows that $H_{y}(x)$ can be made arbitrarily small with a proper encoding procedure. When H(x) > C, then the excess information being pushed onto the channel can only increase the uncertainty $(H_{y}(x))$ of the decoded message. The minimum value of $H_{y}(x)$ is very close to H-C in this latter case.

The computer program in this thesis is implemented with a supplemental segment which stepped through all well-defined convolutional code generators of a specific code rate and



constraint length. Well defined refers to the constraint length definition of the code, meaning that the coefficient of the zero power in the generator polynomial must be set for at least one generator sequence, and then another sequence must have the coefficient set for the K-l power. An example of this is shown here:

n = 2, K = 4;
$$g_1(D) = 1 + D^2$$

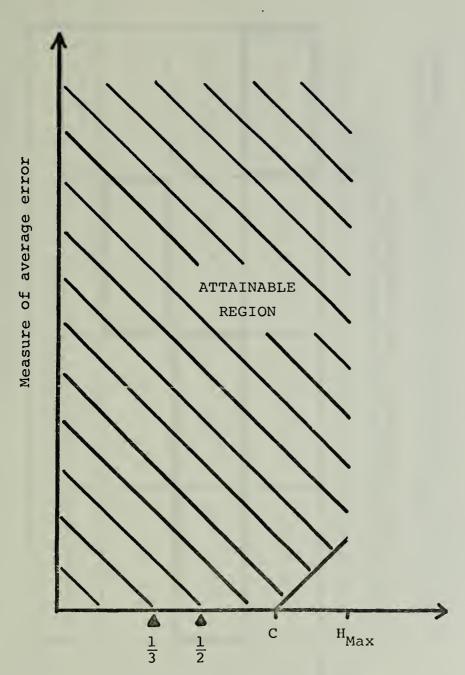
 $g_2(D) = D + D^2 + D^3$
n = 3, K = 3; $g_1(D) = D + D^3 \Rightarrow 1 + D^2$
 $g_2(D) = D^2 + D^3 \Rightarrow D + D^2$
 $g_3(D) = D + D^2 + D^3 \Rightarrow 1 + D + D^2$

The rate is defined by the number of nonzero generator sequences.

The first two paragraphs describe a procedure and the selection of encoders to be processed by the program. The program is applied to find the generator sequences, for a given code rate/constraint length, which come the closest to the lower error $(H_{\hat{Y}}(x))$ boundary of figure 25. Code rates of 1/2 and 1/3 are tested and if the input message is assumed to have 1 bit of information in each bit entering the encoder, then these rates correspond to those plotted on the horizontal scale of figure 25. Tables II through IV present a summary of the test run results for a best code determination.

Each test run was made for a 40,000 bit encoder input applied over various samples of the simulated noise and at





Information Input Rate

C = Channel Capacity $H_{Max} = Maximized H(x)$ at Transmitter

Figure 25. The measure of average error for a given information input rate to a channel (figure is similar to Shannon's Representation).



	0
$\frac{1}{n} = \frac{1}{2}$	ntization
Rate	Ouant

Encoder Constraint Length (K)=3
Decoder Constraint Length (DCL)=16

its)	8.6	5.78 x 10 ⁻¹	5.68 x 10 ⁻¹	4.37 × 10 ⁻¹
λΤ(Channel errors in 16 bits)	4.2	2.4 × 10 ⁻¹	2.74 × 10 ⁻¹	4.68 × 10 ⁻¹
λΤ (Channe	2.0	1.09 x 10 ⁻¹	3.19 × 10 ⁻²	4.67 × 10 ⁻¹
	1.0	5.41 × 10 ⁻²	< 2.5 x 10 ⁻⁵	4.65 x 10 ⁻¹
Generator	Sednences	$\frac{g_1}{g_2} = (100)$	$g_1^{} = (110)$ $g_2^{} = (001)$	$\frac{g_1}{g_2} = (111)$

The probability of decoded bit error = # of message errors 40,000 Note:

The boxes with bold outline contain the minimum error probability determined at the corresponding AT. 2

Results of Test Runs to Determine the Generator Sequences $(n=2,\ K=3)$ Yielding the Minimum Probability of Decoded Bit Error. Table II.



Encoder Constraint Length (K)=4
Decoder Constraint Length (DCL)=16

||

Quantization (Q)

Rate $(\frac{1}{n}) = \frac{1}{2}$

	8.6	5.78 × 10 ⁻¹	5.51 × 10 ⁻¹	4.58 × 10 ⁻¹
rs in 16 bits)	4.2	2.40 × 10 ⁻¹	4.73 × 10 ⁻¹	4.59 x 10 ⁻¹
λT(Channel errors in 16 bits)	2.0	1.09 x 10 ⁻ 1	3.26 × 10 ⁻²	4.59 x 10 ⁻¹
	1.0	5.23 x 10 ⁻²	< 2.5 x 10 ⁻⁵	4.56 x 10 ⁻¹
Generator	Sequence	$\frac{g_1}{g_2} = (1000)$	$g_1 = (1110)$ $g_2 = (0101)$	$g_1 = (1111)$ $g_2 = (1111)$

The probability of decoded bit error = # of message errors 40,000 . H Note:

The boxes with bold outline contain the minimum error probability determined at the corresponding AT. 2

(n = 2, K = 4) Yielding the Minimum Probability of Decoded Results of Test Runs to Determine the Generator Sequences Bit Error. Table III.

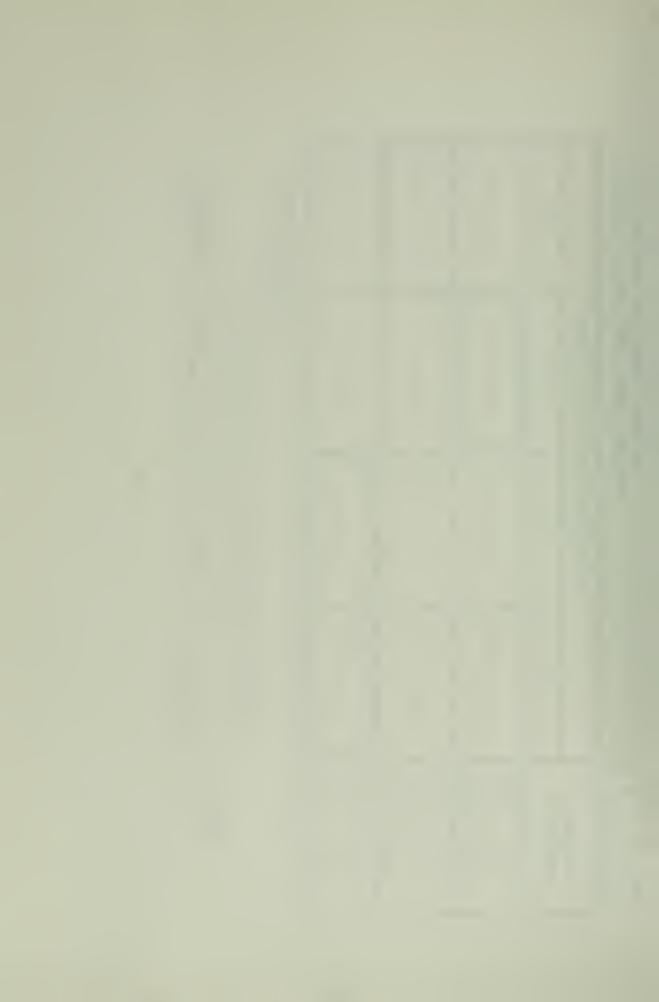


Rate $(\frac{1}{n}) = \frac{1}{3}$ Quantization (Q) = 1

	8.6	5.89 x 10 ⁻¹	4.52 × 10 ⁻¹	6.12 x 10 ⁻¹
cors in 16 bit	4.2	1.35 × 10 ⁻¹	2.23 × 10 ⁻¹	1.6 × 10 ⁻¹
AT (Channel errors in 16 bits)	2.0	2.95 x 10 ⁻²	1.47 × 10 ⁻²	1.65 × 10 ⁻³
	1.0	1.13 × 10 ⁻³	4.74 × 10 ⁻⁵	< 2.5 x 10 ⁻⁵
Generator	Sednences	$\frac{g_1}{g_2} = (100)$ $\frac{g_2}{g_3} = (100)$	$\frac{g_1}{g_2} = (101)$ $\frac{g_2}{g_3} = (101)$	$\frac{g_1}{g_2} = (111)$ $\frac{g_2}{g_3} = (001)$

The probability of decoded bit error = # of message errors 40,000 <u>-</u> Note:

The boxes with bold outline contain the minimum error probability determined at the corresponding AT. Results of Test Runs to Determine the Generator Sequences $(n=3,\ K=3)$ Yielding the Minimum Probability of Decoded Bit Error. IV. Table



four values of $\lambda T(1,2,4,10)$ errors per 16 bits). The computer output is a listing of the decoded message errors for each well defined encoder. This output would require many additional pages to list in this thesis. Therefore, the summary in Tables II through IV is presented instead. The number of decoded errors is then divided by 40,000 to give the measure of average error for each test run (λT).

The various values of λT are obtained by the noise simulation and have the characteristic distributions of those curves presented in figures 18 and 19.

A discussion of these results is presented in part C of this section.

B. DECODER PARAMETER VARIATIONS

In order to provide an insight as to the effects of quantization (Q) and decoder constraint length (DCL), tables V and VI are shown. The effect of increasing Q or DCL is to decrease the frequency of errors thus improving the error correcting scheme. The codes used in these tables are those chosen as the best codes from tables II through IV.

C. DISCUSSION AND CONCLUSIONS

The determination of a best coding scheme for a specific channel application can be made from tables II-IV. The generator sequences which have the minimum frequency of errors (in place of $H_{y}(x)$) for the various values of λT are outlined boldly. Using this comparison technique plus a comparison of the general statistics of the encoder at



other values of λT , the following generator sequences are chosen to be the encoders which meet the criteria set forth previously.

$$N = 2$$
, $K = 3$; $g_1 = (110)$, $g_2 = (001)$
 $N = 2$, $K = 4$; $g_1 = (1110)$, $g_2 = (0101)$
 $N = 3$, $K = 3$; $g_1 = (111)$, $g_2 = (001)$,
 $g_3 = (001)$

These encoders were also used for the results obtained by varying Q and DCL in tables V and VI.

With actual concrete measurements of the effectiveness (minimum error) of a code and a means (computer program) of applying these codes to actual channel recordings there is no reason to have to settle for an inadequate error correcting system. The results presented in this section indicate clear preferences in choosing certain codes to accomplish desired communications in a given noise environment. The user specifics the task and with the computer a code can be chosen. The true value of such a program should be evaluated when implemented with actual channel noise. No one has been able to find a relation or algorithm for encoding that would enable a communication system to reach the maximum average information rate (C) with an arbitrarily small frequency of error. However, computer analysis offers the channel user an opportunity to find a coding scheme which meets the requirements for that channel.

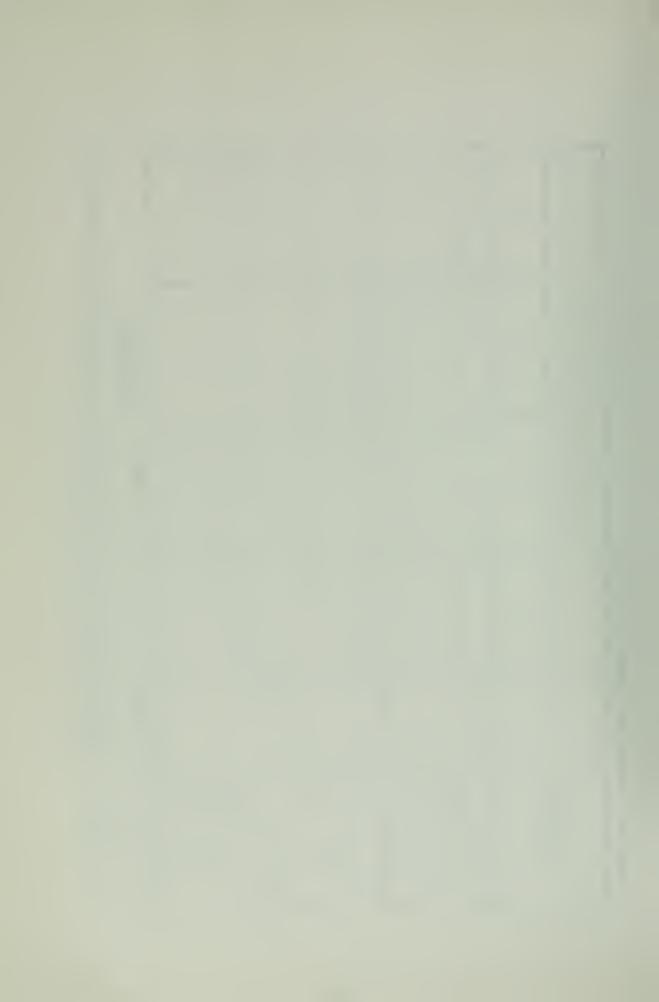


Bits	
16	
li	
Length	
Constraint	
Decoder	

in 16 bits)	4.2 9.8	$2.74 \times 10^{-1} 5.68 \times 10^{-1}$ $6.72 \times 10^{-2} 5.67 \times 10^{-1}$	4.73×10^{-1} 5.51×10^{-1} 8.67×10^{-2} 4.85×10^{-1}	1.6 x 10^{-1} 6.12 x 10^{-1} 2.12 x 10^{-2} 4.75 x 10^{-1}
r (noise errors in 16 bits)	2.0	3.19 × 10 ⁻²	3.26 × 10 ⁻² 1.74 × 10 ⁻⁴	1.65 x 10 ⁻³ < 2.5 x 10 ⁻⁵
λТ	1.0	< 2.5 x 10 ⁻⁵ < 2.5 x 10 ⁻⁵	< 2.5 x 10 ⁻⁵ < 2.5 x 10 ⁻⁵	< 2.5 x 10 ⁻⁵ < 2.5 x 10 ⁻⁵
Ø		3 1	3 3	rt (5
Generator Sequences		$\frac{g_1}{g_2} = (110)$	$g_1 = (1110)$ $g_2 = (0101)$	$\frac{g_1}{g_2} = (111)$ $\frac{g_2}{g_3} = (001)$

The probability of decoded bit error = # of errors 40,000 Note:

Results of Test Runs for Variation in Receiver Quantization (Q) Using the Best Codes from Tables II, III, and IV. Table V.

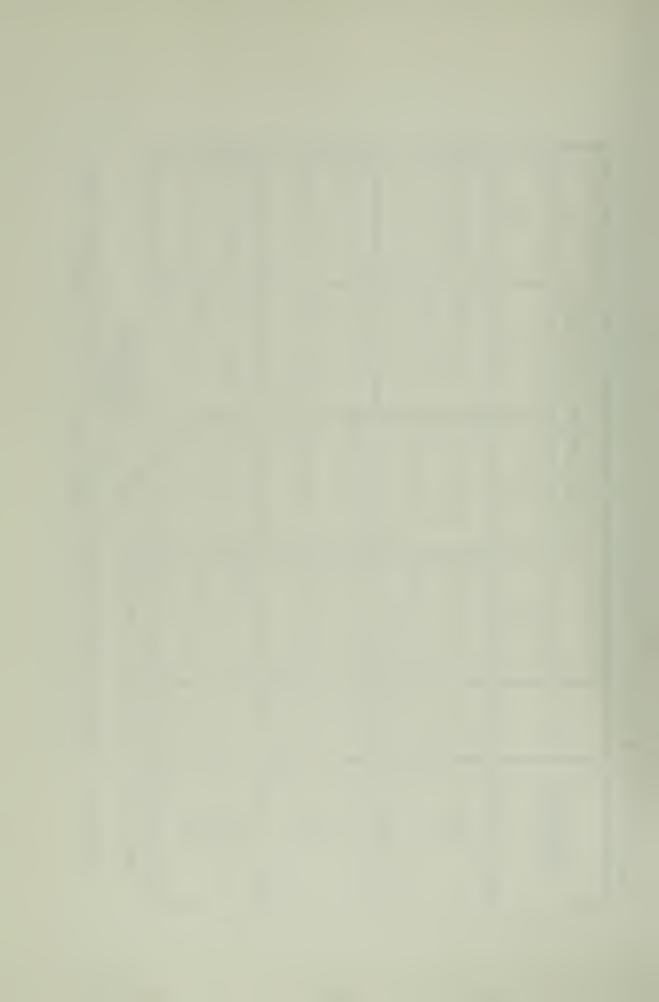


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Generator Sequences 110 001 111 001	DCL 8 8 8 16 16	1.0 x 10 ⁻⁴ 1.0 x 10 ⁻⁵ < 2.5 x 10 ⁻⁵	AT (noise errors in 16 bits) 3.19 x 10 ⁻² 3.19 x 10 ⁻² 2.74 x 10 ⁻¹ 3.19 x 10 ⁻² 4.79 x 10 ⁻¹ 3.26 x 10 ⁻² 1.62 x 10 ⁻¹ 1.65 x 10 ⁻³ 1.65 x 10 ⁻³ 1.65 x 10 ⁻³ 1.65 x 10 ⁻³	s in 16 bits) 2.74 × 10 ⁻¹ 2.74 × 10 ⁻¹ 4.79 × 10 ⁻¹ 4.73 × 10 ⁻¹ 1.62 × 10 ⁻¹ 1.6 × 10 ⁻¹	5.68 × 10 ⁻¹ 5.68 × 10 ⁻¹ 5.50 × 10 ⁻¹ 6.20 × 10 ⁻¹ 6.12 × 10 ⁻¹
--	--------------------------------	---	---	---	---

The probability of decoded bit error = # of errors 40,000 Note:

Results of Test Runs for Variation in Decoder Constraint Length (DCL) Using the Best Codes from Tables II, III, and IV. Table VI.



APPENDIX A

POSITION INDEPENDENT CODE CORE MAP

THE CORE LOCATIONS OF ADDRESSES, COUNTERS, AND MISCELLANEOUS STORAGE (WORK) AREAS ARE LISTED BELOW.

SOME OF THESE VALUES, PRECEDED BY *, ARE ENTERED BY OR COMPUTED BY THE PROGRAM INITIALIZATION SUBPROGRAM, WHICH FOLLOWS THE INPUT SUBPROGRAM.

- * 13600; INPUT BLOCK ADDRESS
- 13602; ENCODED/DECODED BLOCK ADDRESS
- 13604; QUANTIZED CODE SEQUENCE BLOCK ADDRESS.
- * 13606; NOISE SEQUENCE BLOCK ADDRESS
- 13610; RANDOM NUMBER/PERTURBED SEQUENCE BLOCK ADDRESS
- * 13612; TRELLIS TABLE BLOCK ADDRESS
- 13614; SSEQ(I) TABLE BLOCK ADDRESS
- * 13616; SCORE(I) TABLE BLOCK ADDRESS
- * 13620; SSEQ(J) TABLE BLOCK ADDRESS
- * 13622; SCORE(J) TABLE BLOCK ADDRESS
 - 13624; "NOT USED"
- * 13626; GENERATOR SEQUENCE BLOCK ADDRESS
- * 13630; STACK ADDRESS
 - 13632; HOLD (STORAGE)
 - 13634; DELTA (USED IN DECODER)
 - 13636; MASK (USED TO MAKE DECODED BIT DECISION)
 - 13640; WORK (STORAGE)
 - 13642; MESSAGE WORD (16 BITS) COUNT WORK LOCATION
 - 13644; MQ BIT COUNT WORK LOCATION



- 13646; DECODED BIT COUNTER
- 13650; NUMBER OF SCORES COUNTER
- 13652; MINIMUM SCORES ADDRESS
- 13654; MINIMUM SCORE VALUE
- 13656; N-BIT LOOP COUNTER
- 13660; ZERO BIT SCORE VALUE
- 13662; ONE BIT SCORE VALUE
- 13664; SSEQ WORK LOCATION
- 13666; TOTAL OF NOISE VALUES IN NOISE SEQUENCE
- 13670; TOTAL NUMBER OF ERRORS IN NOISE SEQUENCE
- 13672; TOTAL NUMBER OF DECODED MESSAGE BIT ERRORS
- 13674; "NOT USED"
- 13676; "NOT USED"
- 13700; NUMBER OF CODE BITS PER INPUT BIT, N
- * 13702; ENCODER CONSTRAINT LENGTH, K
- * 13704; QUANTIZATION VALUE, Q
- * 13706; DECODER CONSTRAINT LENGTH, DCL
 - 13710; MESSAGE WORD (16 BITS) COUNT, W
- * 13712; POWER OF TWO USED IN GENERATING NOISE SEQUENCE
- 13714; OPERATION (DIVIDE/MULTIPLY) USED FOR NOISE
- 13716; Q X N
- * 13720; Q X N X W
- * 13722; 4 X K (NONZERO STATES INITIAL SCORE)
- * 13724; 2 ** K
- * 13726; (2 ** K) 1
- * 13730; 2 ** (K 1)
- * 13732; (2 ** (K 1)) 1



- * 13734; 2 ** (K 2)
- * 13736; (2 ** Q) 1
- * 13740; DCL + K 1
- * 13742; 2 ** (DCL 1)
- 13744; SCORE(I) SSEQ(I) (SUBTRACT ADDRESSES)
- 13746; SSEQ(J) SSEQ(I) (SUBTRACT ADDRESSES)
- * 13750; N X W
 - 13752; NEXT SCORE ADDRESS
 - 13754; NEXT SSEQ ADDRESS
 - 13756; STORAGE LOCATION FOR A COUNTER VALUE OF 2
 - 13760; G(1), GENERATOR SEQUENCE
 - 13762; G(2), GENERATOR SEQUENCE
 - 13764; G(3), GENERATOR SEQUENCE
 - 13766; G(4), GENERATOR SEQUENCE
 - 13770; G(5), GENERATOR SEQUENCE
 - 13772; G(6), GENERATOR SEQUENCE
 - 13774; G(7), GENERATOR SEQUENCE
 - 13776; G(8), GENERATOR SEQUENCE

THE WORD COUNT IN LOCATION 13710 IS PLACED THERE BY AN INSTRUCTION AT THE END OF THE MESSAGE INPUT SUB-PROGRAM. THE VALUE OF THE GENERATOR SEQUENCES IS ENTERED BY THE PROGRAMMER BEFORE STARTING A RUN.



APPENDIX B

PROGRAM LISTING OF NOISE SIMULATION

The following flow chart depicts the flow of the instructions in the following machine language listing of the noise simulation subprogram. The numbers (base 8) on the upper left of the blocks in the flow chart correspond to those instruction addresses of the subprogram mentioned in that block.



(11200-11324)

This segment quantizes the encoded block, that is, encoded 1's become Q 1's and encoded 0's become Q 0's. The result is then placed in block specified at (13604).

(11330-11374)

This segment generates the random number sequence by the Lehmer Congruential Relation. These numbers are stored in a block beginning at the address specified at (13610).

(11376-11546)

This segment uses the noise parameters placed in locations (10230) and (10236) to change the value of the number of set bits in a 16 bit random number, so that the density of errors (λT) in the noise is varied. The noise sequence is stored in a block beginning at an address in (13606).

(11550-11646)

This segment determines the noise value total (13666) and the number of errors (13670) for a given message, i.e., a value ≥ 4 is an error for Q=3.

(11650-11700)

This segment adds the noise block to the quantized block and stores the result in a perturbed block beginning at an address in (13610)

END OF SUBPROGRAM



The following computer printout is the noise program just discussed.

011200	7016700	011330	7016700
011202	7002376	011332	7002254
011204	7016701	011334	7012701
011206	7002374	011336	7004704
011210	7016702	011340	7012702
011212	7002534	011342	7000401
011214	7022767	011344	7012737
011216	7000001	011346	7044444
011220	7002462	011350	7177304
011222	7001003	011352	7010237
011224	7012021	011354	7177306
011226	7077202	011356	7005237
011230	7000436	011360	7177304
011232	7012703	011362	7013720
011234		011364	7177304
011236	7012704	011366	7077107
011240	7000020	011370	7010067
011242	7016705	011372	7002300
011244	7002436	011374	7000240
011246	7006310	011376	7005067
011250	7103405	011400	7002264
011252	7006311	011402	7005067
011254	7005303	011404	7002262
011256	7001410	011406	7016700
011260	7077504	011410	7002176
011262	7000416	011412	7016701
011264	7006311	011414	7002170
011266	7005211	011416	7012703
011270	7005303	011420	7000020
011272	7001406	011422	7012704
011274	7077505	011424	7000020
011276	7000410	011426	7012006
011300	7005721	011430	7020067
011302	7012703	011432	7002240
011304	7000020	011434	7001003
011306	7000764	011436	
011310	7005721	011440	7002146
011312	7012703	011442	7012006
011314	7000020	011444	7005005
011316	7000766	011446	7006206
011320	7077430	011450	7005505
011322	7005720	011452	7077403
011324	7077234	011454	7005767
011326	7000000	011456	7002234



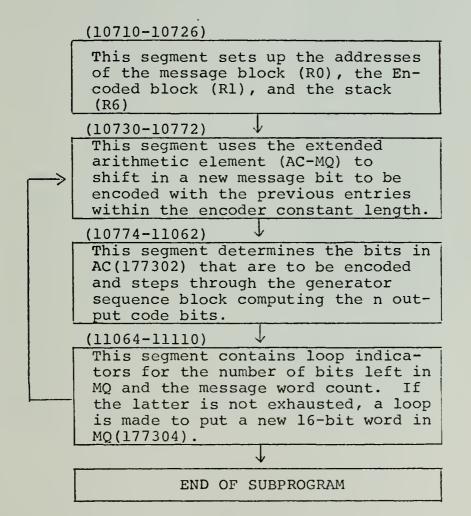
011460	7001005		011574	7006305
011462	7016704		011576	7006304
011464	7002224		011600	7005505
011466	7006205		011602	7005302
011470	7077402		011604	7001413
011472	7000407		011606	7077306
011474	7016737		011610	7060567
011476	7002212		011612	7002052
011500	7177304		011614	7016703
011502	7010537		011616	7002116
011504	7177306		011620	7006203
011506	7013705		011622	7020503
011510	7177304		011624	7003760
011512	7005303		011626	7005267
011514	/002405		011630	7002036
011516	7006311		011632	7000755
011520	7005305		011634	7012004
011522	7003373		011636	7012702
011524	7005211		011640	7000020
011526	7000735		011642	7077117
011530	7005721		011644	7000240
011532	7020167		011646	7000240
011534	7002052		011650	7016700
011536	7001001		011652	7001732
011540	7000403		011654	7016701
011542	7012703		011656	7001724
011544	7000017		011660	7016702
011546	7000763		011662	7001724
011550	7016700		011664	7016705
011552	7002032		011666	7002030
011554	7016701		011670	7012003
011556	7002140		011672	7012104
011560	7012702		011674	7074304
011562	7000020		011676	7010422
011564	7012004		011700	7077505
011566	7016703		011702	7000000
011570	7002112		ਮ :	
011572	7005005			



APPENDIX C

Program Listing of Rate 1/n Convolutional Encoder

The following flow chart depicts the flow of the rate 1/n convolutional encoder implementation. The corresponding machine language program follows the flow chart and the instruction addressed are indicated on top of the respective flow chart block to which they correspond in the subprogram.





The following computer printout is the encoder implementation just discussed.

010710	7016700	011012	7012302
010712	/002664	011014	7040502
010714	7016701	011016	7005046
010716	/002662	011020	7016746
010720	7012704	011022	7002656
010722	7000020	011024	7005726
010724	/016706	011026	7006202
010726	7002700	011030	7005516
010730	7016716	011032	7005346
010732	7002754	011034	7001373
010734	/012037	011036	7006311
010736	7177304	011040	
010740	7005037	011042	7006226
010742	7177302	011044	7005511
010744	/000406	011046	7005304
010746	7013746	011050	7001003
010750	7177302	011052	7012704
010752	/012037	011054	7000020
010754	/177304	011056	7005721
010756	/012637	011060	7005316
010760	/177302	011062	7001353
010762	7012746	011064	7005726
010764	/000020	011066	7005316
010766	/012737	011070	7001336
010770	7000001	011072	7005726
019772	/177314	011074	7005316
010774	7015746	011076	7001323
010776	7002700	011100	7005704
011000	7013705	011102	7001403
011002	7177302	011104	
011004	7016703	011106	7005304
011006	7002616	011110	7001375
011010	7005105	011112	7000000



APPENDIX D

Program Listing of Viterbi Decoder

The following flow chart depicts the flow of the Viterbi decoding algorithm implementation. The corresponding machine language program follows the flow chart and the instruction addresses are indicated on top of the respective flow chart block to which they correspond in the subprogram.



(11710-12042)

COMPUTE TRELLIS AND STORE IN TRELLIS BLOCK (13612).

(12044-12146)

QUANTIZE TRELLIS TABLE ENTRIES FOR Q > 1

(12150 - 12206)

INITIALIZE SSEQ(I) (13614) AND SCORE (I) (13616)

(12210−12366)<

DECODE OLDEST BIT IN THE SSEQ(I) SEQUENCE WITH THE MINIMUM SCORE

(12370 - 12546)

SHIFT INTO MQ(177304)
N BITS FROM THE PERTURBED
SEQUENCE (13610)

(12550-12772)

COMPUTE & BETWEEN THE N-BIT INPUT AND EACH N-BIT BRANCH CODE. ADD THE BRANCH & TO IT CORRESPONDING PRESENT SCORE. DETERMINE THE BRANCH WITH THE MINIMUM SCORE ENTERING EACH NEXT STATE.

(12774-13072)

CHANGE EACH SSEQ CORRESPONDING TO THE BIT LOST FROM THE PRESENT STATE

(13074-13166)

 $I \longleftrightarrow J$

(*)



The following computer printout is the decoder implementation just discussed.

	7016700	012056	7016701
	7002014	012053	2 /001650
011714	7016701	012054	7016702
011716	7001706	012056	7001550
011720	7016702	012066	7016703
011722	7001666	912962	2 /001614
011724	7016704	012064	7016704
011726	7001700	012066	7001614
011730	7005003	012076	
011732	7005012	012073	2 /006210
011734	7016714	012074	/ /103403
011736	7001740	012076	7006312
011740	7005103	012100	0 /077402
011742	7012105	01210	2 /000403
011744	7040305	01210	1 /006312
011746	7016744	01210	7005212
011750	7001730	012110	0 /077403
011752	7005006	01211	2 /005742
011754	7006205	01211	7077315
011756	7005506	012116	3 /005722
011760	7005314	012120	0 /016703
011762	7001374	01212	2 /001554
011764	7006312	01212	1 /005010
011766	7006206	01212	5 /016704
011770	7005512	01213	0 /001552
011772	7005724	01213;	2 /006310
011774	7005314	01213	1 /077402
011776	7001361	01213	
012000	7016701	01214	
012002	7001622	01214	
012004	7005722	01214	
012006	7005103	01214	
012010	7026703	01215	
012012	7001712	01215	
012014		01215	
	7020300	01215	
012020	7002002	01216	0 /016702
012022	7060003	01216:	
012024	7000742	01216	
012026	7160003	01216	
012030	7005203	01217	
012032	7000737	01217	
012034	7022767	01217	
012036	7000001	01217	
012040	7881642	01220	
012042	7001442	012207	
012044	7016700	01220	
012046	7001542	01220	5 /077404



012210	7016701	012350	7005367
012212	7001400	012352	7001272
012214	7016702	012354	7001012
012216	7001376	012356	7005724
012220	7016704	012360	7005367
012222	7001356	012362	7001256
012224	7001336	012364	7001003
012226	7001460	012366	/000000
012230	7001400	012370	7000240
012232	7001410	012372	7000240
012234	7000020	012374	7012767
012236	7001404	012376	7000020
012240	7012337	012400	7001244
012242	7177304	012402	7010102
012244	7012767	012404	7066702
012246	7000020	012406	7001334
012250	7001374	012410	7005037
012252	7005367	012412	7177302
012254	7001462	012414	7016706
012256	/002051	012416	7001276
012260	7016767	012420	7012737
012262	7001444	012422	7000001
012264	7001362	012424	7177314
012266	7010267	012426	7005367
012270	7001360	012430	7001212
012272	7012267	012432	7001402
012274	7001356	012434	7077607
012276	7005367	012436	7000414
012300	7001346	012440	7012767
012302	7001405	012442	7000020
012304	7021267	012444	7001176
012306	7001344	012446	7013767
012310	7002766	012450	7177302
012312	7005722	012452	7001156
012314	7000770	012454	7012337
012316	7166767	012456	7177304
012320	7001422	012460	7016737
012322	7001326	012462	7001146
012324	7016706	012464	
012326	7001322	012466	7000762
012330	7006314	012470	7016767
012332	7036716	012472	7001240
012334	7001404	012474	7001160
012336	7100004	012476	7010267
012340	7000240	012500	7001250
012342	7000240	012502	7010167
012344	7000240	012504	7001246
012346	7005214	012506	7020267



012510 /	001106	(012650	7000240
012512 7		6	112652	7066767
012514 /		(312654	7000756
012516 /			12656	7001000
012520 /			312660	
012520 7			012662	
			312664	
012524 /				
012526 /			312666	
012530 /			012670	
012532 /				7017767
012534 /			012674	
012536 /				7000762
012540 /			312700	
012542 /				7000774
012544 /			012704	
012546 /			012706	
012550 /				7000726
012552 /	/000002		012712	
012554 4	/001200		312714	
012556	/011267	(312716	7000720
012560 /	/001076		312720	7005067
012562 4	7016706		312722	7000710
012564	/001112	(312724	7005167
012566	/013767	(312726	7000710
012570	/177302		012730	7016705
012572			312732	
012574				7016767
012576			012736	
012600				7000674
	/005067		012742	
	/001026		012744	
	/005167			7000666
	7003107 7001026			7066767
	7001020 7016705		012752	
012614				7000005
012614				7000636
	7010707 7001114		012736 012760	7000267
	_			
	7001012		012762	7077503
	7046767		012764	7077617
	7001010		012766	7066767
	7001004		012770	7000642
	7066767		012772	7000666
	7001000		012774	7026767
	7000774		012776	7000660
	7006267		913000	7000660
	7000774		013002	7003421
012644	7077503		013004	7016705
012646	7077617	1	013006	7000742



7016715		013100	7010667
7000646		013102	7000650
7010167		013104	7005367
7000644		013106	7000646
7066767		013110	7001222
7000704		013112	7022122
7000636		013114	7000240
7016705		013116	7005367
7000632		013120	7000534
7016706		013122	7001212
7000716		013124	7016700
		013126	7000462
		013130	7020267
		013132	7000464
			7100406
			7016701
			7000452
			7016702
			7000450
			7162707
			7000700
			7016701
			7000442
			7016702
	•		7000440
			7000714
7000652		013166	7000000
	/000646 /010167 /000644 /066767 /000704 /000636 /016705 /000632 /016706	/000646 /010167 /000644 /066767 /000704 /000636 /016705 /000716 /011516 /006316 /006316 /006705 /000700 /016705 /000776 /016715 /000576 /011116 /006316 /016705 /016705 /016705 /016705 /010560 /016705 /016705 /016705 /016705 /016705 /016705 /016705 /016705 /016705 /016705 /016705	7000646 013102 7010167 013104 7000644 013106 7000704 013112 7000636 013114 7000632 013120 7016706 013122 700716 013124 7005216 013130 7005216 013132 700700 013134 7016705 013142 700700 013134 7016715 013142 7016716 013144 7016705 013150 7016706 013142 7016707 013140 7016706 013142 7016707 013140 7016706 013142 7016707 013140 7016706 013142 7016707 013140 7016708 013140 7016709 013140 7016709 013140 7016709 013140 7016709 013140 7016709 013140 7016709 013140 7016709 013140



APPENDIX E

Program Listing of Supplementary Subprograms

1. Initialization subprogram (10174-10706)

This subprogram enters the necessary addresses and constants into those locations noted in Appendix A by *.

The computer listing below is the initialization subprogram.

010174	7010700	
010176	7012767	
010200	7000002	
010202	7003474	
010204	7012767	
010206	7000003	
010210	7003470	
010212	7012767	
	7000001	
	7003464	
	7012767	
	7000020	
	7003460	
	7012767	
	7000001	
	7003456	
	7012767	
	7000000	
010240		
010242		
010244		
	7003514	
	7010167	
010252	7003352	
010254		
	7000406	
	7010167	
	7003344	
	7062700	
010266	7003402	

010270 /010001 010272 /062700 010274 /000600 010276 /010021 010300 /066700 010302 /003404 010304 /010021 010306 /016737 010310 /003366 010312 /177304 010314 /016737 010316 /003370 010320 /177306 010322 /013767 010324 /177304 010326 /003420 010330 /063700 010332 /177304 010334 /010021 010336 /016737 010340 /003342 010342 /177306 010344 /013767 010346 /177304 010350 /003346 010352 /063700 010354 /177304 010356 /010021 010360 /063700 010362 /177304



010364	/010021	010536	7016702
010366	/063700	010540	7003142
010370	/177304	010542	7005003
010372	7010021	010544	7005203
010374	7005002	010546	7006303
010376	7005202	010550	7077202
010400	7016703	010552	7005303
010402	7003276	010554	7010367
010404	7006302	010556	7003156
010406	/077302	010560	7005203
010410	7010267	010562	7006203
010412	7003310	010564	7010367
010414	7006302	010566	7003106
010416	7060200	010570	7016702
010420	/010021	010572	7003106
010422	7006202	010574	
010424	/005302	010576	7066702
010426	7010267	010600	
010430	/003274	010602	7010267
010432	/005202	010604	7003132
010434	7012703	010606	7016702
010434	/000003	010610	
010436	/060200 /060200	010612	70053074
010442	7010021	010614	
010444	/077303	010616	7005203
010446	707505	010620	7005203
010450	7010267	010622	7077202
010452	7003254	010624	
010454	/005302	010626	7003112
010456	7010267	010630	7016702
010460	/003250	010632	7002764
010462	/005202	010634	
010464	7006202	010636	7002756
010466	7010267	010640	
010470	7003242	010642	7003100
	7012737	010644	
010474	7000004	010646	7002752
010476	7177304	010650	7156702
010500	7016737	010652	7002742
010502	7003176	010654	7010267
010504	7177306	010656	7003066
010506	7013767	010660	7010700
010510	7177304	010662	7062700
010512	7003206	010664	7001364
010514	7016737	010666	7010067
010516	7003164	010670	7002304
010520	7177304	010672	7006267
010522	7016737	010674	7003012
010524	7003152	010676	7006267
010526	7177306	010700	7003016
010530	7013767	010702	7006267
010532	7177304	010704	7003042
010534	7003160	010706	7000000



2. Message Input Subprogram (10000-10144)

This subprogram was used to indicate that an alphanumeric symbol typed at the Keyboard was entered into core (echo). The symbols are stored in core in an ASC II (7-bit) code representation. The Keyboard symbol, @, is used to terminate message entry and the number of 8-bit computer bytes used is stored in location (13710 Appendix A). The following computer printout is a listing of the ASC II message input subprogram.

010000 /010700 010064 /000012 010002 /062700 010066 /105737 010004 /004376 010070 /177564 010006 /005002 010072 /100375 010010 /105737 010074 /112737 010012 /177560 010076 /000200 010014 /100375 010100 /177566 010016 /113710 010102 /077107 010020 /177562 010104 /105737 010022 /122710 010106 /177564 010024 /000300 010110 /100375 010026 /001435 010112 /112737 010030 /105737 010114 /000212 010032 /177564 010116 /177566 010034 /100375 010120 /000733 010036 /112037 010122 /012703 010040 /177566 010124 /000010 010042 /005202 010126 /105020 010044 /123727 010130 /005202 010046 /177562 010132 /077303 010050 /000215 010134 /006202 010052 /001356 010136 /006302 010054 /112740 010140 /010267 010056 /000240 010142 /003544 010060 /105720 010144 /000000 010062 /012701



3. Message Output Subprogram (13200-13364)

This subprogram is basically the same as that in section 2 of this appendix. However, besides typing what is in core starting at a location specified at (13602), the number of errors (bit differences) are determined between the input message and the decoded out message.

This message error value is stored at (13672) (Appendix A).

The following computer printout is a listing of the ASC II (7-bit) code output subprogram.

013200	7016700	013274	7100375
013202	7000376	013276	7112737
013204	7012701	013300	7000012
013206	7000040	013302	7177566
013210	7111037	013304	7105737
013212	7177566	013306	7177564
013214	7122720	013310	7100375
013216	7000000	013312	7000734
013220	7001435	013314	7000240
013222	7105737	013316	7000240
013224	7177564	013320	7016700
013226	7100375	013322	7000254
013230	7005301	013324	7016701
013232	7100366	013326	7000252
013234	7122710	013330	7005002
013236	7000240	013332	7011003
013240	7001363	013334	7074311
013242	7112737	013336	7012704
013244	7000015	013340	7000020
013246	7177566	013342	7006211
013250	7012702	013344	7005502
013252	7000012	013346	2077403
013254	7105737	013350	7022021
013256	7177564	013352	7020067
013260	7100375	013354	7000224
013262	7105037	013356	7001365
013264	7177566	013360	7010267
013266	7077206	013362	7000306
013270	7105737	013364	7000000
013272	7177564	*	



4. Analysis Subprograms (13250-13544)

From address (13250) to address (13376) a short subprogram is listed that is used to step through well defined
encoders of rate 1/2, 1/3, and 1/4. In the last addresses
(13400-13544) a program is listed which determines the
number of error bits in 16-quantized bits and stores the
results so that a distribution of errors may be plotted
as in figures 17-23. (See next page.)



		01	3400	7016700
			3402	7000202
			3404	7016701
			3406	7000326
013250	7005267		3410	7006201
013252	7000512		3412	7000201
013254	7026727		3414	7000240
013256	7000506		3416	7000020
013260	7000010		3420 3420	7000020
013262	7001030		3422	7000214
013264	7012767		3424	7014100
013266	7000004		3426 3426	7014100
013270	7000474		3430 3430	7000020
013272	7005267		3432 3432	7000020
013274	7000466		3434 3434	7000240
013276	7026727			
013300	7000462		3436	7000240
013302	7000010		3440	7000240
013304	7000018		3442	7005006
013306	7001017		3444	7016703
013310			3446	7000234
	7000004		3450	7005002
013312	7000450		3452	7006302
013314	7005267		3454	7006310
013316	7000442	_ ···	3456	7005502
013320	7026727		3460	7005367
013322	7000436	01	3462	7000152
013324	7000020	01	3464	7001407
013326	7001006	01	3466	7077307
013330	7012767		3470	7020201
013332	7000010	01	3472	7003401
013334	7000424	01	3474	7005206
013336	7062767	61	3476	7005305
013340	7000002	. 01	3500	7001414
013342	7000414	01	3502	7000760
013344	7016777	81	3504	7005720
013346	7000322	01	3506	7026700
013350	7000416	01	3510	7000076
013352	7062767	91	3512	7002003
013354	7000002		3514	2000000
013356	7000410	01	3516	7000240
013360	7026727		3520	7000240
013362	7000374		3522	7012767
013364	7000021		3524	7000020
013366	7001402		3526	7000106
013370	7000137		3530 3530	7000756
013372	2010000		3532	7006306
013374	7000137		3534	7060604
013376	7001172		3536 3536	7005004
			3540 3540	7000214
			3542	7000270
			3544	7000000
		01	2044	7 000000



APPENDIX F

SAMPLE RUN

THE COMPUTER LISTING BELOW THIS PARAGRAPH IS A DEMONSTRATION OF THE PROCEDURE REQUIRED TO USE THE ENTIRE PROGRAM PROPERLY. THE PROGRAM IS STORED ON A DISK UNDER THE NAME VSAC, SAV. THE CONVOLUTIONAL CODE USED IS A RATE 1/2 (K=3) CODE. OTHER INPUTS ARE Q=1, DCL=16 (20 IN BASE 8), AND THE GENERATOR SEQUENCES OF 3 AND 4 (BASE 8).

^ C

. GET VSAC, SAV

.START 1172 ODT V01-01

:

- *10200/0000002
- *10206/000003 *10214/000001
- *102147000000
- *10222/000020
- *10230/000001
- *10236/000001
- *
- *12336/100004
- 4
- *13760/000003
- *13762/0000004
- **3**}:
- ** ^* C
- .START 10000



The paragraph below is the input message for the sample run.

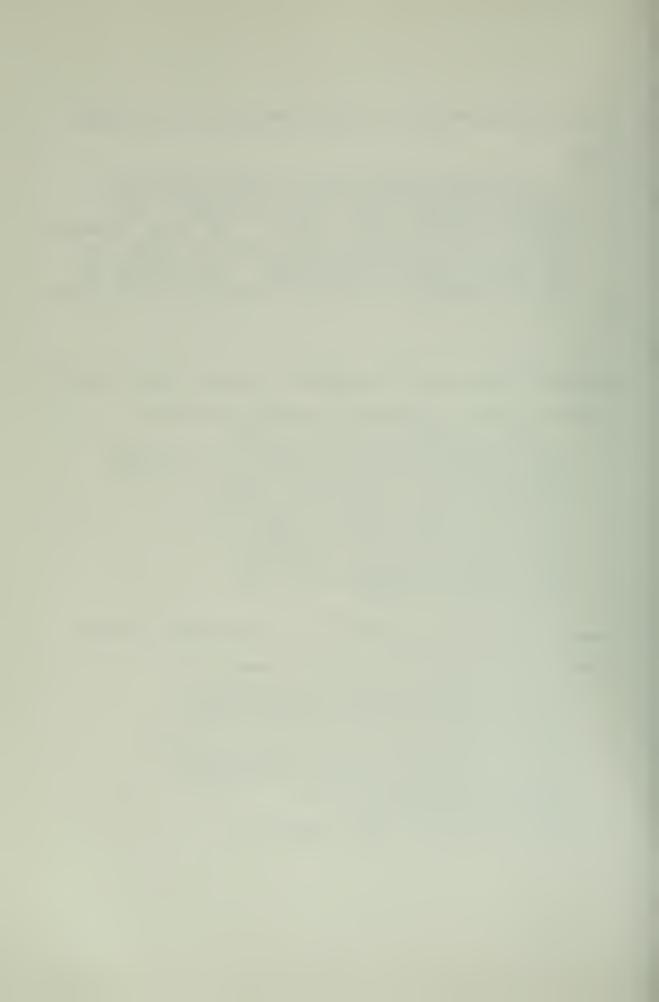
THIS IS A SAMPLE RUN OF A THESIS COMPUTER PROGRAM USED TO EVALUATE THE PERFORMANCE OF RATE 1/N CONVOLUTIONAL CODES, OVER A SIMULATED NOISY CHANNEL, WITH A VITERBI DECODER. THE NOISE PARAMETERS FOR THIS RUN (CORE LOCATIONS 10230 AND 10236) ARE THE SAME AS WERE USED TO OBTAIN THE DISTRIBUTION IN FIGURE 20 OF THE THESIS TEXT. THIS MESSAGE WILL NOW BE TERMINATED BY THE 'AT' CHARACTER ON THE PANEL.

When the message above is encoded (as given above) and the noise is added, the resulting decoded message is:

THIS IS!A"SOMPLE RUN OF E THESIS
COMPUTE PROGRAM USED NO EVALUATE
THE ERFNRUANCE@OF RATE 1/N CONVOLUTIONAL!@CDES,
OVMR APIMULBTEE NOISY PANNEL ITH(@
VITERBI DECOLDR. UHE NOISE PARAMETERS
FOR TPIS UN (COU LOCATIONS 10230
AND 102361 ARU \$E SAUA AS TEVE USED"TO
OBTAIN THE @ISTRIBUTION INOFJURE
21 OF THE THEIP TEXD. THIS MESSAGD
NILL NIN BE TERMINATED BY"THM 'AX'
CHBRCTER ON THM @BNE@.

When no coding is applied to the input message and the same noise is added the received message is:

* Improper carriage return received.



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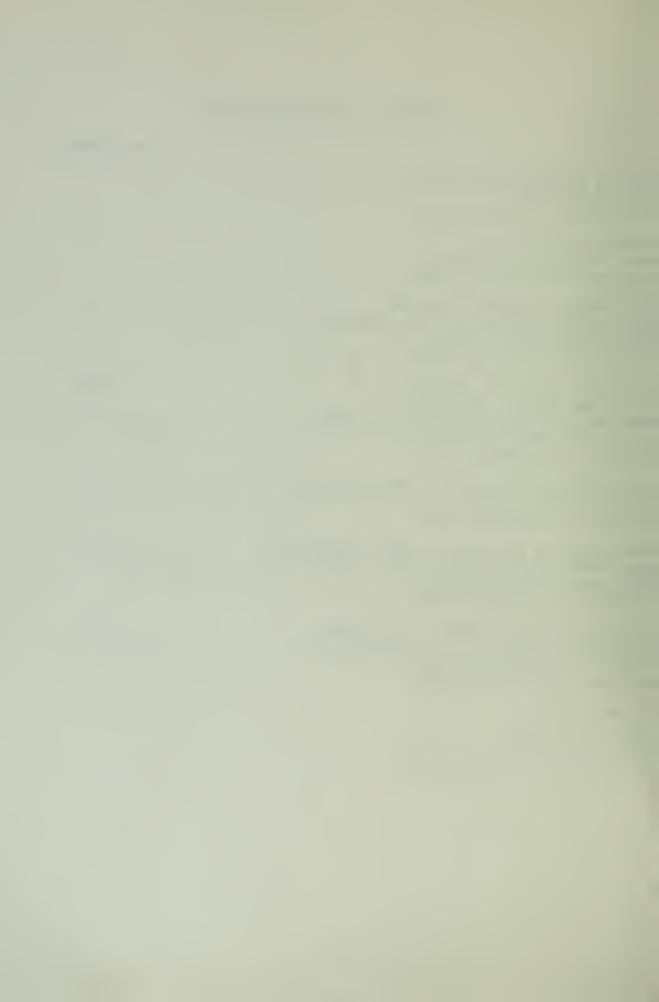
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 No. 2, pp. 260-269, April 1967.
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A comparison of rational over a simulated noist terbi decoding algorite Bibliography: l. 9 Thesis (M. S. in E. School, 1974. 156333

Thesis

H193 Haney

c.1 A comparison of rate 1/n convolutional codes over a simulated noisy channel using the Viterbi decoding algorithm.

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A comparison of rate 1/n convolutional c

3 2768 001 01764 3
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